Technology and Cost Trends at Advanced Nodes

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Who we are

- IC Knowledge LLC is the world leader in cost modeling of semiconductors and MEMS.
- Our customers are the worlds largest IDMs, fabless companies, foundries, and system, equipment and materials companies.
- Our models are all detailed bottoms up models:
  - We have follow the latest trends in technology to build the process flows.
  - We estimate costs for existing processes and future processes and technologies.

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Outline

- Logic Technologies
  - Defining a node
  - Technology trends
  - EUV impact
  - Costs
  - Embedded MRAM
- DRAM – scaling issues
- 3D NAND – 2D to 3D transition
- 3D Xpoint – where it fits

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Logic nodes

- ASML has analyzed logic nodes versus contacted poly half-pitch (CPHP) and minimum metal half-pitch (MMHP):

$$\text{Standard Node} = 0.14 \times (\text{CPHP} \times \text{MMHP})^{0.67}$$

Applying the ASML formula to IC Knowledge data results in the following table:

	32nm/28nm	22nm/20nm	16nm/14nm	10nm	7nm	5nm
Global Foundries	25	NA	17	NA	9.2 (2017?)	7.1 (2019?)
Intel	31	21	13	9.5 (2017)	5.9 (2020)	2023?
Samsung	27	20	17	12 (2016)	9.2? (2018)	7.1 (2020?)
TSMC	27	18	18	12 (2016)	9.2 (2017)	7.1 (2019?)

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Source: ASML formula, IC Knowledge data

Foundry node scaling challenges

- 10nm (12nm standard node)
  - Short lived half node for TSMC. Longer lived and more variants for Samsung.
  - Scaling will provide density and performance advantages.
  - Contact resistance optimization and side wall spacer k value reduction.
- 7nm (9.2nm standard node)
  - Hard to scale performance.
  - Likely cobalt filled vias and contacts.
  - Possibly SiGe PMOS channel for performance.
  - Samsung says they will do EUV at 7nm
- 5nm (7.1nm standard node)
  - Very hard to scale performance with FinFETs.
  - Likely SiGe PMOS channel or switch to horizontal nanowires (HNW).
  - Likely EUV introduction but don’t want to do HNW at the same time.
  - Possible half node shrink with EUV prior to HNW introduction?

Foundry roadmap example - TSMC

	28nm	20nm	16nm	10nm	7nm	5nm	3.5nm
Year	2011	2014	2015	2016	2017	2019	2022
Transistor	Planar	Planar	FinFET	FinFET	FinFET	FinFET	HNW
Channel (NMOS/PMOS)	Si/Si	Si/Si	Si/Si	Si/Si	Si/Si	Si/SiGe	Si/Si
Threshold voltages	4	4	5	5	5	5	3-4
Metal layers	10	10	11	12	13	14	15
Contact and Via – Interconnect	W – Cu/Ta/TaN	W – Cu/Ta/TaN	W – Cu/Ta/TaN	W – Cu/Ta/TaN	Co – Cu/Co/TaN	Co – Cu/Co/TaN	Co – Cu/Ru/TaN
Strain	DSL, eSiGe, SM	DSL, eSiGe, SM	eSiGe	eSiGe	eSiGe	eSiGe	eSiGe?
CPP (nm)	113	90	90	64	54	44	**32**
MMP (nm)	90	64	64	42	38	32	**24**

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After 3.5nm we expect a stacked horizontal nanowire technology to provide density scaling

EUV

- Will not be the single exposure all critical layers technology it was once expected to be. Will be introduced for selected layers.
- Implementation in order:

1. Single exposure for contact/vias to replace LE3/LE4.
2. SAQP with multiple block masks for metal is very complex – SAQP with single EUV block is very attractive.
3. Possibly in the front end for SAQP with single EUV cut.

- Mask defect issues may initially limit it to low open area masks.
- At 5nm, without EUV increases wafer cost 6%, cycle time by 20%, capital cost by 6% and fab size by 12% (assuming 100 wph for EUV - lower than ASML's target) [1].

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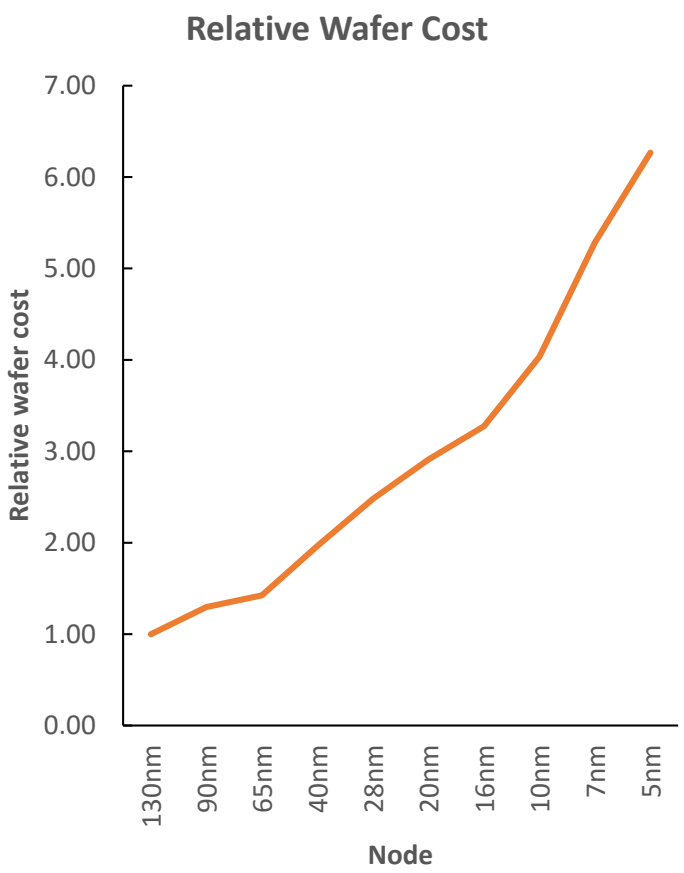
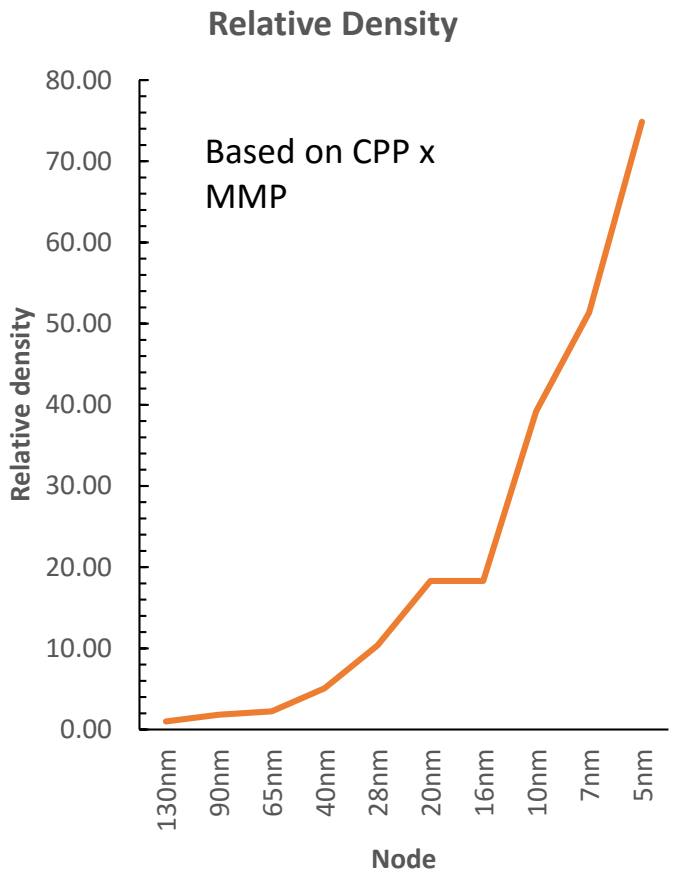
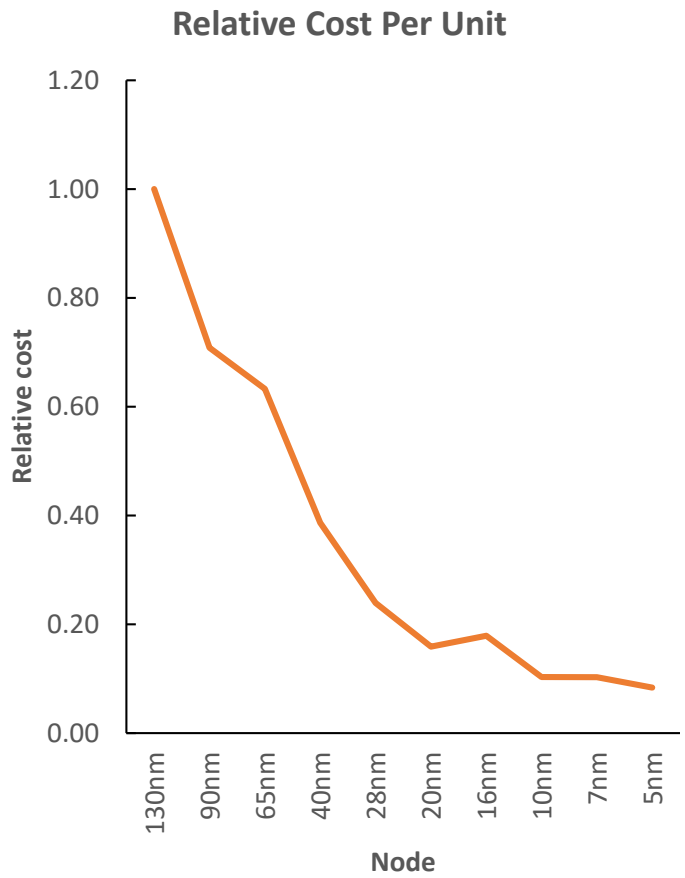
[1] IC Knowledge – Strategic Cost Model

Cost impact example - TSMC







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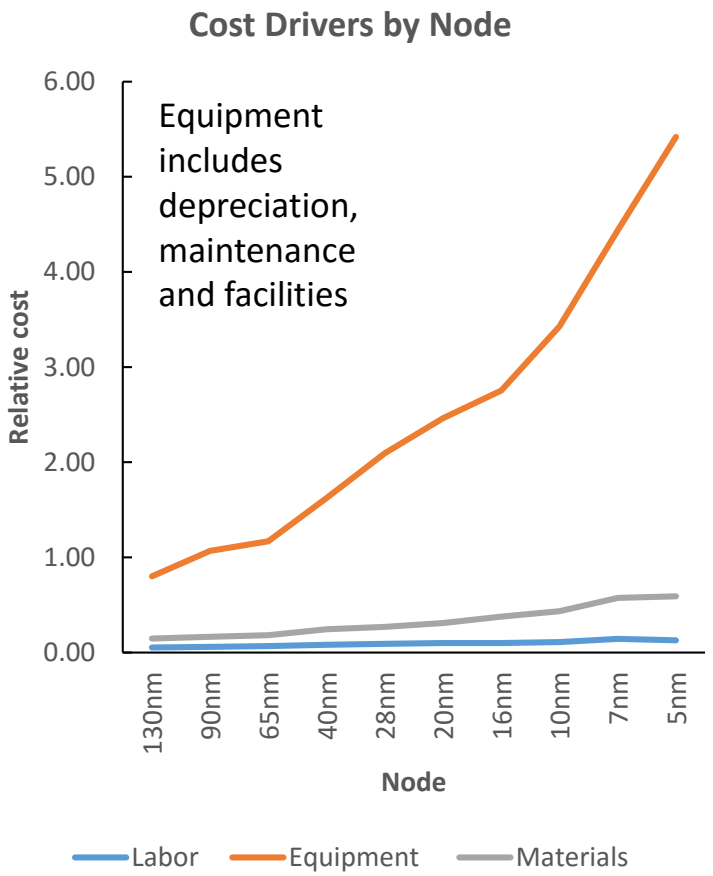
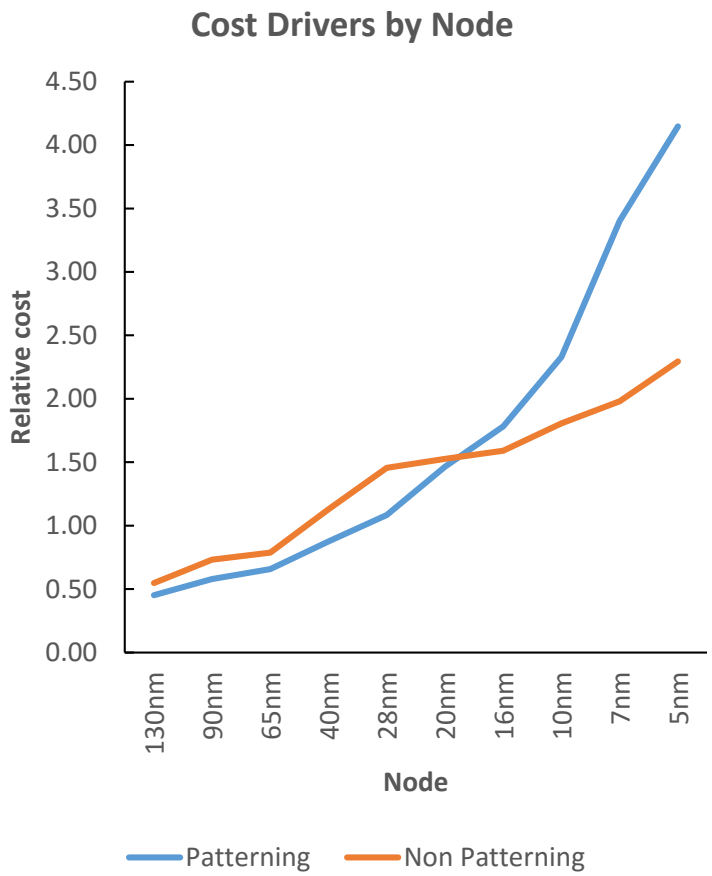
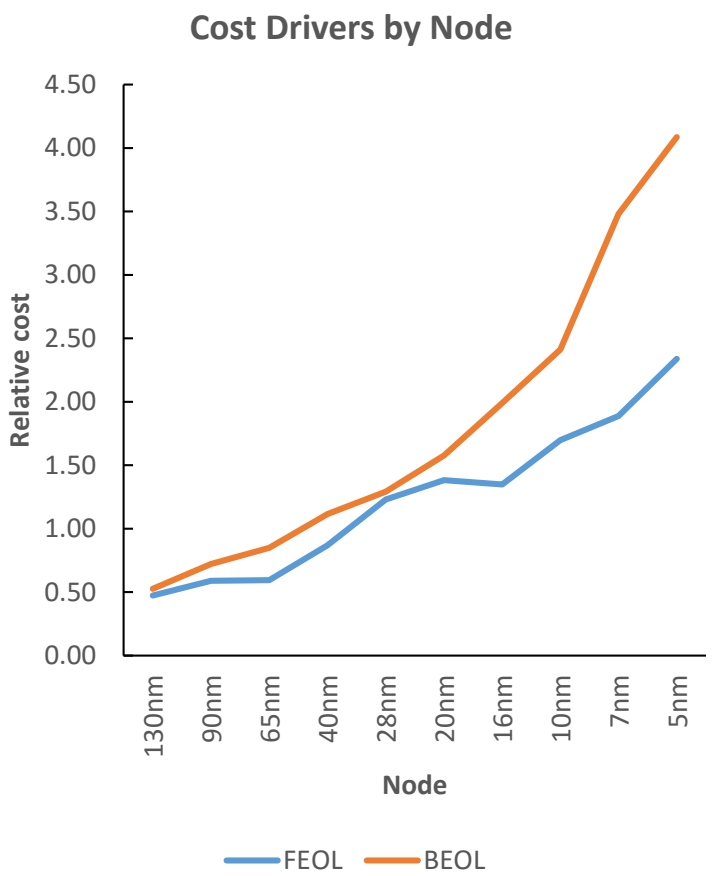
Source: IC Knowledge – Strategic Cost Model

Cost breakout example - TSMC







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Source: IC Knowledge – Strategic Cost Model

MRAM opportunity

- Modern processor architectures include registers and L1, L2 and L3 cache on-chip.
- Cache can easily exceed 50% of the area of an SOC design.
- Currently registers and cache are typically 6T SRAM.
- STT MRAM is a 1T1R cell with the memory cell in the interconnect layers. A 4x or more reduction in area versus SRAM is possible.
- STT MRAM could potentially replace upper level cache.
- We estimate that an STT MRAM module added to a 16nm process adds ~6% to the cost [1].

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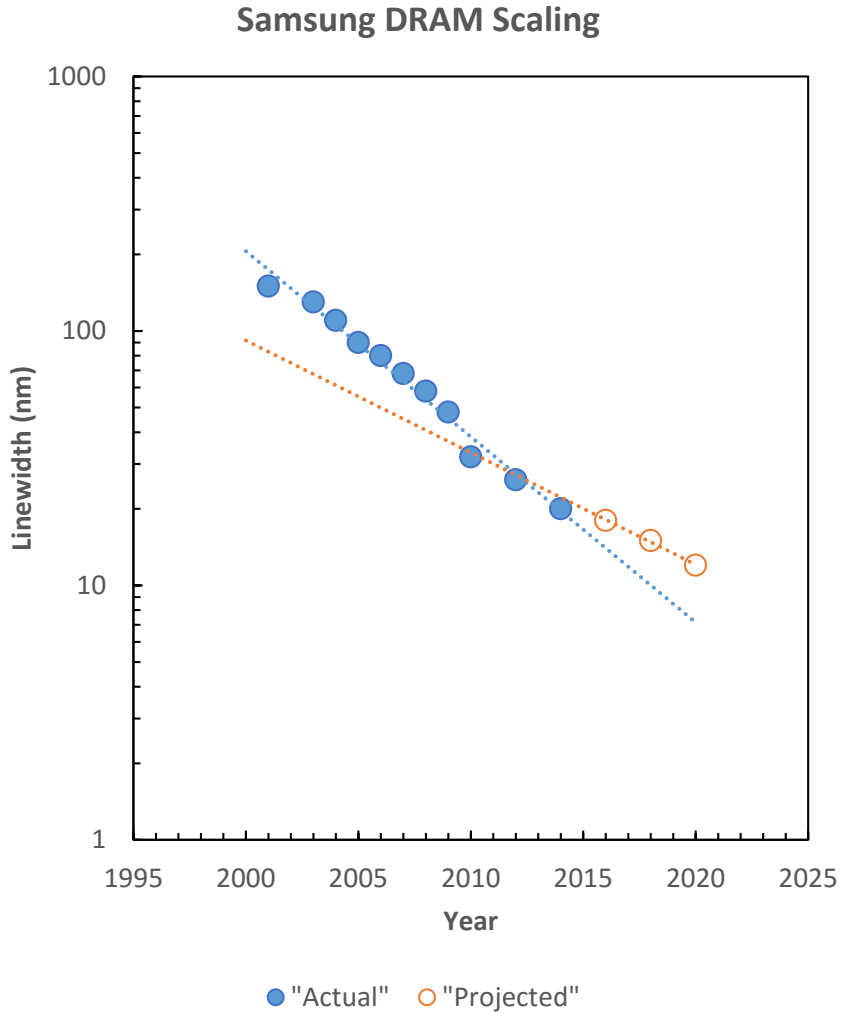
[1] IC Knowledge – Strategic Cost Model

DRAM scaling example - Samsung

- Capacitor issues have slowed scaling – higher k materials = higher leakage.
- There are opportunities in the periphery to manage lower capacitance, to lower parasitics and provide higher drive current with FinFETs and HKMG or improved metals.
- Longer term some type of multi-level STT MRAM may replace DRAM.
- STT MRAM has the endurance and speed but hasn't reached the density yet – 3D?



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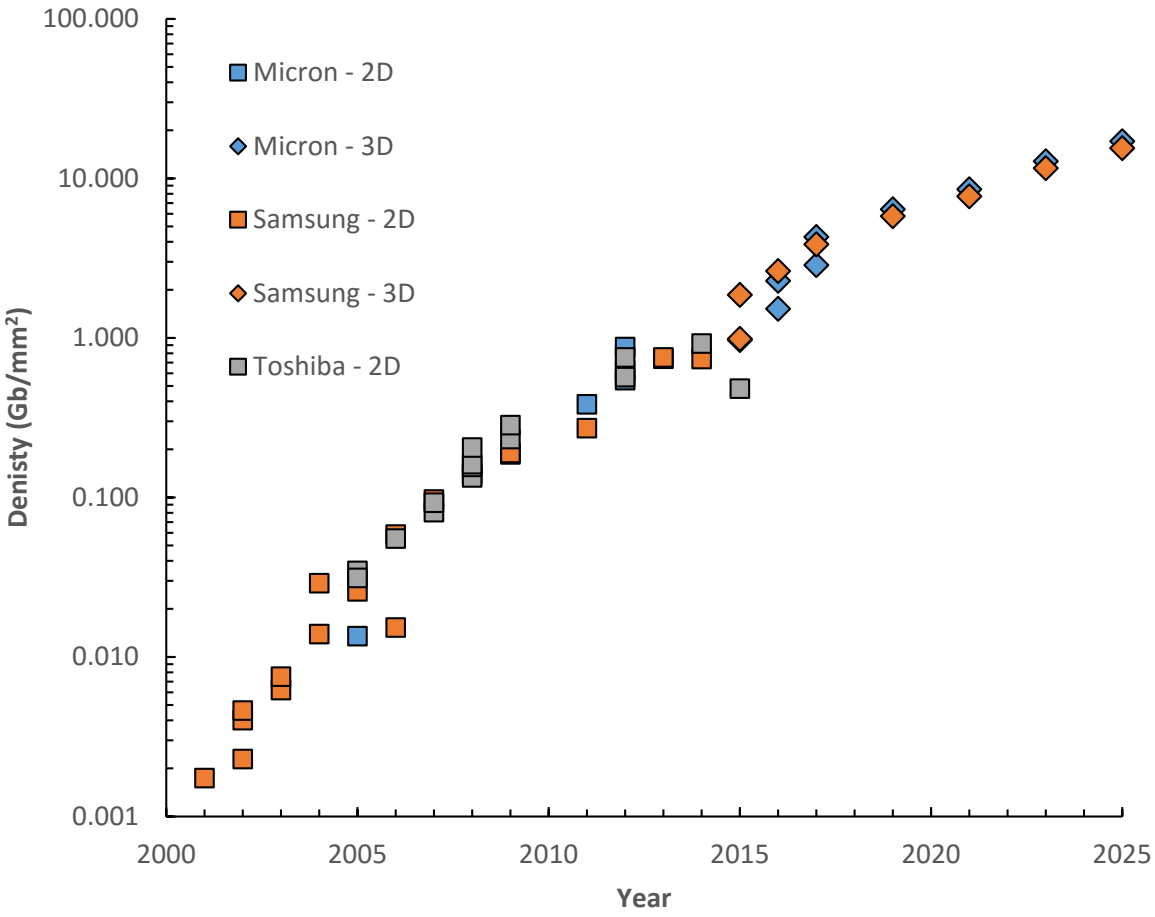
3D NAND – scaling in the third dimension

- 2D NAND scaling beyond 16nm/15nm is uneconomical.
- 3D NAND adds additional layers for scaling in place of 2D lithographic scaling.
- Bit density is continuing to scale with the potential for terabit NAND die.



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3D NAND roadmap example – Intel-Micron

Year	2016	2017	2019	2021	2023
Stacks	1	2	2	2	3
Layers per stack	32	32	48	64	64
Total layers	32	64	96	128	192
Bits/cell	2/3	2/3	3	3	3
Channel type	Poly	Poly	Poly	High mobility	High mobility
Peripheral logic	CMOS under	CMOS under	CMOS under	CMOS under	CMOS under
Density (Gb/mm2)	1.52/2.28	2.86/4.29	6.40	8.54	12.80

- CMOS under the memory array increases the percentage of the die area that is memory array but increases the stress in the memory array (Intel-Micron are currently the only producer with CMOS under).
- As stack layers increase channel mobility becomes and issue and alternative materials such asInGaAs will be required.

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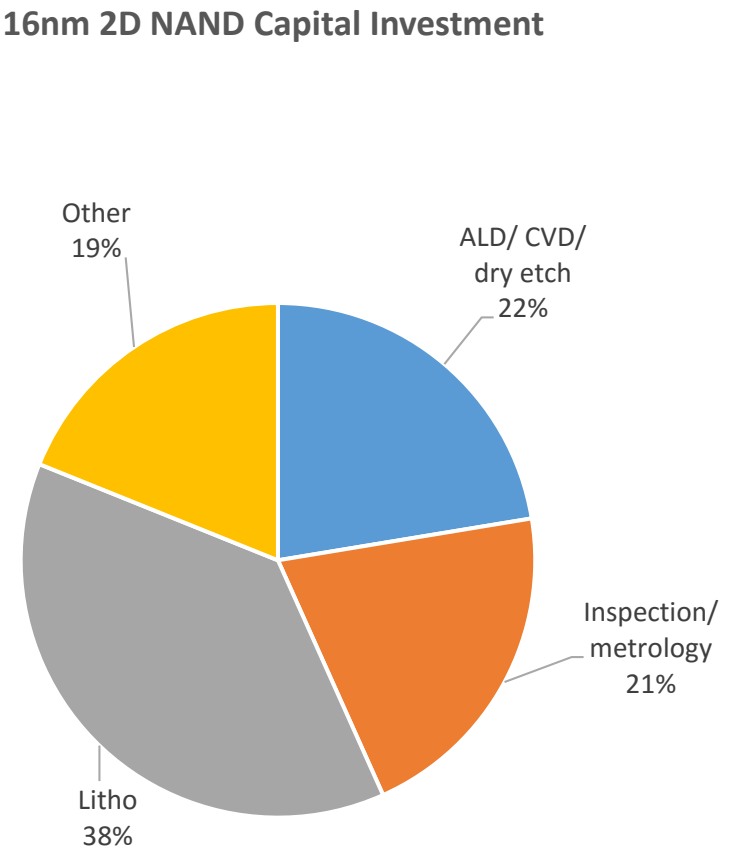
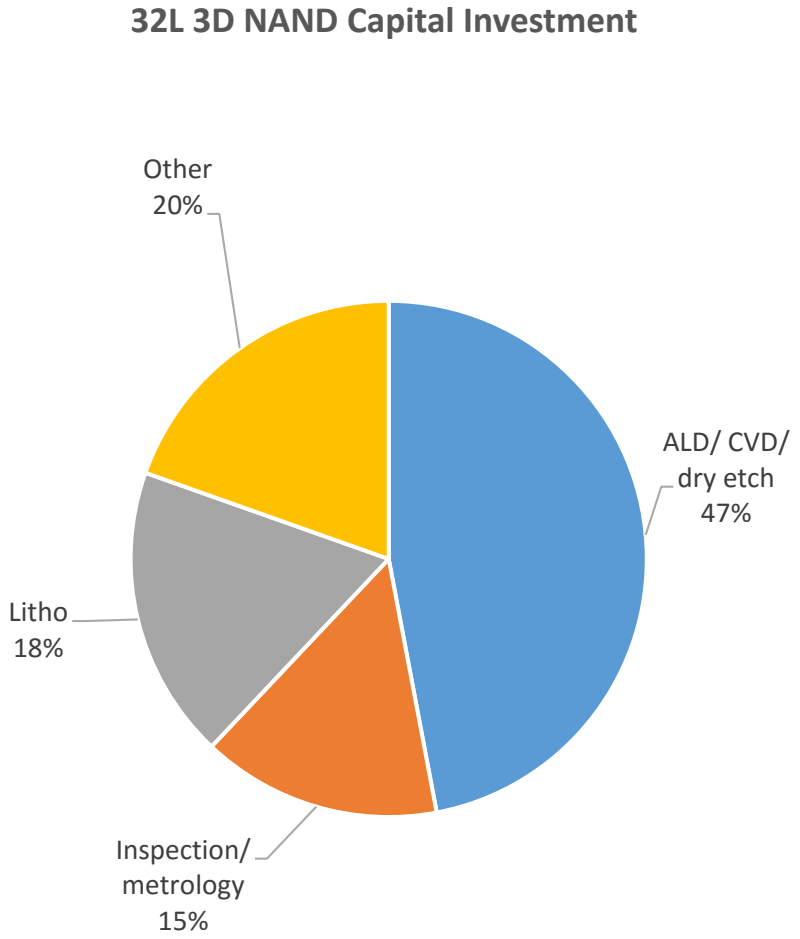
2D NAND to 3D NAND equipment impact





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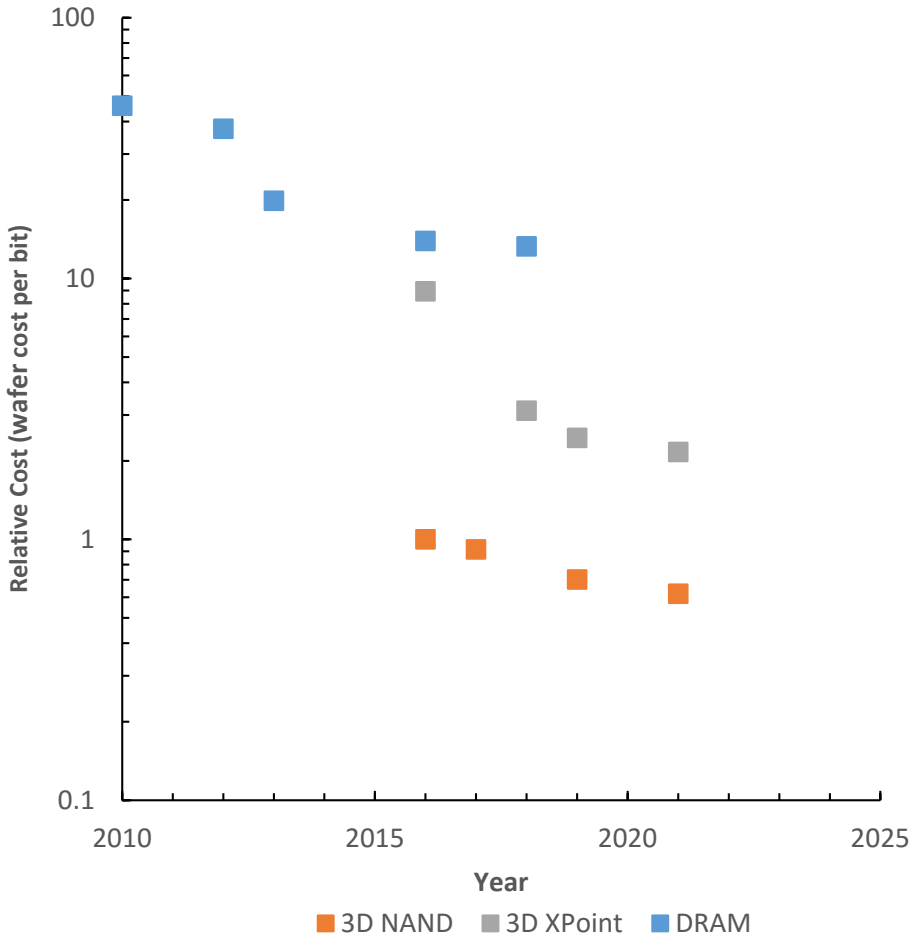
Source: IC Knowledge – Strategic Cost Model

3D XPoint

- Introduced by Intel-Micron (SanDisk is pursuing an RRAM alternative).
- The memory array is 2 layers and we believe the memory array is 2x nm over a 3x nm logic process.
- We believe the memory is a PCM memory cell with an Ovonics Transfer Switch selector.
- We believe the 2 layer memory cell requires 7 double patterned mask layers.
- Scaling can be by additional memory layers, lithography shrinks or transitioning from single bit to multi-bit memory.
- Our primary roadmap is based on adding layers and multi-bit capability, we are still evaluating options.

3D XPoint cost versus 3D NAND and DRAM

- 3D XPoint is faster than NAND but slower than DRAM.
- 3D XPoint has better endurance than NAND but not good enough to replace DRAM.
- 3D XPoint is higher cost than 3D NAND cost and we believe this will continue to be the case.
- 3D XPoint will be a complimentary technology to 3D NAND and DRAM utilized for Storage Class Memory.



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Conclusion

- Logic has a scaling path well into the 2020s with a transition to horizontal nanowires and 3D stacked horizontal nanowires.
- DRAM scaling has slowed with a possible long term 3D STT MRAM transition.
- 3D NAND is positioned to scale into the 2020s with terabit memories on the horizon.
- 3D XPoint is a complementary technology to DRAM and 3D NAND for storage class memory applications.
- 3D everything is the future of leading edge.