IC Cost and Price Model User Manual

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Version 2019 model

Introduction

This manual presents an overview of IC Cost and Price Model and the basic workings of the model. Revision 01 refers to the 1st revision of the manual, it does not indicate a model revision the manual applies to.

Model description

The IC Cost and Price Model is designed to easily calculate the cost and price of most low power silicon ICs. Examples of low power ICs include microcontrollers, microprocessors, FPGAs, low power ASICs, DRAM, Flash, SRAM, etc. The model does not cover any non-silicon based ICs and does not cover power ICs or discrete devices, these are covered by separate models. The IC Cost and Price model processes are limited to low power processes such as CMOS, BiCMOS, RFCMOS, DRAM, NAND, NOR, SRAM, etc. BCD and HVIC coverage is provided by our Discrete and Power Products Cost and Price Model. Specialized power IC and discrete device packages are also not covered by the IC Cost and Price Model. Power packages are covered in our Discrete and Power Products Cost and Price Model. The IC Cost and Price Model is also limited to past and current processes and processes expected to be introduced to production within the next year. Nodes not expected to be introduced in the next year are covered in our Strategic Cost Model that covers logic processes out to the 2.5nm node and memory processes out to the 10nm node. The IC Cost and Price Model provides some approximate values for equipment and materials requirements but for exact and detailed equipment and materials requirements the Strategic Cost Model should be utilized.

Please note that our cost models are cost of goods sold (COGS) models and do not include below the line costs such as research and development (R&D) or selling, general and administration costs (SG&A). Our pricing calculations are cost plus gross margin (GM). R&D and SG&A costs are absorbed in GM as well as profits.

Support and updates

As a licensee to the IC Cost and Price Model you will receive all updates made to the model for twelve months from the date of purchase emailed to your email address of record. If you change your email address it is your responsibility to notify us. Reasonable levels of phone and email support will be provided for twelve months from the date of purchase of the model. On-site or other forms of support are not provided. For more information, please see our Support Policy.

Our "Support Policy", "Add process request form" and other support items for this model are available in the grey bar on the right side of the IC Cost Model page on our web site here: http://www.icknowledge.com/products/icmodel.html

Known Excel bugs and limitations

- We occasionally see issues with dropdown menus not working properly in the model. If you click on a dropdown menu and can't see the dropdown list, right click in the cell, choose "Pick from Drop Down list" and then left click in the cell and the dropdown should appear. This is an Excel bug and not something we can address ourselves.
- Number formatting must use a decimal point to indicate decimals, e.g. 1.0. If you set up Excel to use a coma to indicate a decimal, e.g. 1,0 the model will not function correctly. This setting is an Excel option under advanced and you can set "Use system separators" for a "Decimal separator" to be a . or ,. It is common practice in Europe to use a , but that will prevent the model from working correctly.
- We use a lot of dropdown lists in the model. Excel 2007 does not support dropdown lists that reference other sheets in the model. We have currently designed the model to work around this issue but at some point we will cease to support Excel 2007 because there is a lot of overhead involved in accommodating this.

Model conventions

There are several conventions used throughput the model.

The gray areas on each model sheet contain the model inputs and outputs. The inputs that can be directly changed by the user are white areas within the gray, the gray areas are labels and model driven outputs and cannot be directly changed by the user.

Throughout the model there are red dots indicating comments. Moving the cursor over the red dots displays information explaining input or outputs.

In this manual, regular, bold and underlined text describe the model and model features. Italic text provides background on the inner workings of the model.

Common Questions

- How do I model an SOC - we get this question a lot. There is a perception that SOC specifies what something is, it doesn't. SOC stands for System On a Chip and is vaguely defined industry buzz word that can be applied to many different types of devices. Things like cell phone applications processors are commonly referred to as SOCs, but most microprocessors, most microcontrollers and many other products meet the definition of SOC as well. You can model an SOC in the model but you need to model the product based on what it is.
- What package do I select for Chip Scale Packages (CSP) - this is similar to SOC described above, CSP basically means a package is roughly the size of the die or chip it contains. Many package types can be CSPs, simply select the package type of interested, BGA, QFN, etc.

Worksheet overview

The following is a brief description of the model worksheets and the purpose of each sheet. The sheet tabs are color coded, gray is informational (these sheets may in some cases be editable but do not drive the model results), red are the main drivers (these sheets are editable), brown are results (these sheets are not editable), blue modifies the processes or performs comparisons or calculations (these sheets are editable).

Please note that there are many sheets in the model and scrolling between them can be a slow process. If you right click in the area where the scrolling arrows are (bottom left part of Excel) you will get a sheet list and you can directly select the sheet you want to go to.

- License (Gray tab) – the model software license. This sheet is not editable.
- Introduction (Gray tab) – a brief introduction to IC Knowledge and our cost modeling product line as well as disclaimer and warrantee information. This sheet is not editable.
- HELP (Gray tab) – a listing of the various ways to get help with the model. This sheet is not editable.
- Main Selections (red tab) – the 5 selections required to build a model are on this sheet. This is the main driver of model results. This sheet is user editable.
- Defaults (red tab) – this sheet displays the default values for all of the model defaults and allows the user to override them. This sheet is user editable.
- Cost Summary (brown tab) – the main summary of the cost model results including wafer, test and packaging cost. This sheet is not user editable.
- Cost Per Quarter Macro (brown tab) - this sheet will display a summary of costs by quarter for twenty quarters once you run the macro.
- Foundry Margin (brown tab) - when a foundry process is selected this sheet displays a graph of foundry margin versus volume. This sheet is not user editable.
- Lookups (gray tab) – lookup tables to help the user make selections on the 'Main Selections' tab. This sheet is user editable.
- Errors (gray tab) – this sheet provides details about any errors that occur in the model. This sheet is not user editable.
- Process adders (blue tab) – allows the user to add various process blocks to the base process. This sheet is user editable.
- Multiple die (blue tab) – this worksheet allows costs for multiple die in a single package to be calculated. This sheet is user editable.
- Wafer Cost Detail (brown tab) – this worksheet displays detailed information about the wafer cost. This sheet is not user editable.
- Revision History (Gray tab) – this worksheet displays the revisions made to the current year's model along with details of what the changes were. This sheet is not user editable.
- Blank 1 (gray tab) - an unlocked worksheet for user calculations and note. This sheet is user editable.
- Blank 2 (gray tab) - an unlocked worksheet for user calculations and note. This sheet is user editable.
- Blank 3 (gray tab) - an unlocked worksheet for user calculations and note. This sheet is user editable.
- Lists (gray tab) – lists of the numeric values that correspond to each model input setting. These values are useful when driving the model from the 'Override' worksheet. This sheet is user editable.

- Override (red tab) – this worksheet allows the user to drive the model from their own calculations. This sheet is user editable.

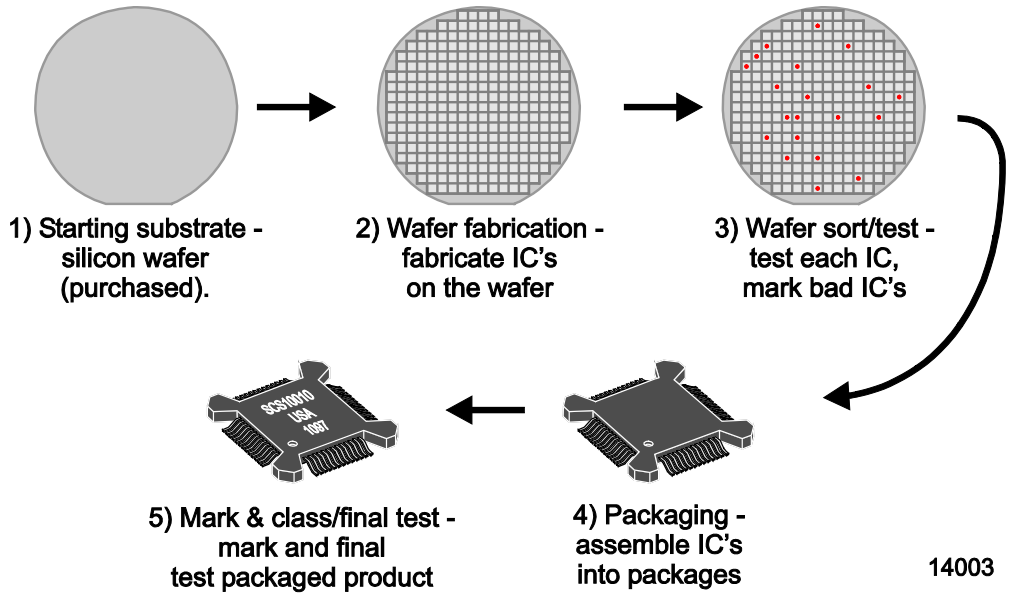
Detailed worksheet descriptions

In this section the “active” worksheets are described in more detail. Worksheet such as ‘License’, ‘Introduction’, ‘Help’, ‘Revision History’, ‘Lists’ and the blank worksheets are expected to be self-explanatory.

Background – The IC Manufacturing Flow

The following are the main steps in the IC manufacturing flow:

- *Starting wafer – this is purchased by all IC manufacturers. Wafers come in a variety of sizes and types. When you select a process the appropriate wafer size and type is automatically selected.*
- *Wafer fabrication – anywhere between tens to tens of thousands of integrated circuits are fabricated on the surface of the wafer. The wafer yield is the number of wafers that complete fabrication process divided by the number of wafers started into the fab.*
- *Wafer sort (also called wafer test or wafer probe) – the ICs on the wafer surface are tested and the bad ICs are mark with an ink dot or in an electronic map so they won't be packaged. Die yield is the number of die that pass wafer sort divided by the total number of die on the wafer. Wafer sort may be a single pass test or may include multiple passes at different temperatures, or before and after bakes and burn-ins.*
- *Packaging – the individual ICs on the wafer are cut up and put into protective packages that provide electrical connections to the IC.*
- *Class test (also called final test) – the packaged ICs are tested to insure the ICs were correctly packaged without damage. For some ICs they can't be fully tested until they are packaged and this may be the first full test. Class test may be a single pass test or may include multiple passes at different temperatures, or before and after bakes and burn-ins.*



IC Manufacturing Flow

Main Selections (red tab)
This is the main sheet driving the model.

At the top of the sheet (row 6) next to the words “Model inputs (you must select all of these)” is a box that displays error messages if an error occurs. If an error message appears here please go to the ‘Errors’ sheet to learn more about the error. If an error is present you do not have a valid model and the error must be fixed. The most common error is to select a process that isn’t on-line yet on the date selected in the ‘1 Select year and quarter to model’. If that is the error message, simply select a later date to model until the error message goes away. Other errors will require you to contact IC Knowledge to get them resolved.

Row 7 has a box that will display an informational message if any defaults are overridden or any process adders are in use. This is not an error message but rather just information to make sure you don’t have a default overridden or a process adder active without realizing it.

1.0) Select year and quarter to model (cell C8) – this should be when the parts were made or when you expect them to be made if you want to project cost and price over time. The year and quarter to model affects labor and utility rates, material costs, and packaging costs on a yearly basis and depreciation and die yield on a quarterly basis. You should select the year and quarter your parts were manufactured. It is a good practice to also model plus or minus two quarters to see if there is a large change due to depreciation. When segments of a wafer fab equipment set become fully depreciated you may see large drops in cost. The exact dates equipment become fully depreciated have some uncertainty and by looking forward and backwards two quarters you can evaluate the uncertainty.

2.0) Select process to model (cell C9) – this is the most fundamental selection in the model and drives the process, the wafer fab the process is run in, labor and material costs and many other factors. The resulting wafer cost will be displayed in cell K11.

An example of a process is: 300mm – 28nm – TSMC – HP (G) – CMOS – DGO, HKMG – 1P/11Cu. The nomenclature is wafer size (300mm) – node (28nm) – company (TSMC) – process name (HP (G)) – process type (CMOS) – process details (DGO, HKMG) – Fab name (optional) - poly/metal layers and type (1P/11Cu). For a process where any of the entries don’t apply NA is used for not applicable.

The abbreviations used in the process list are:

Process Type

- BCD = Bipolar, CMOS and DMOS – being removed on 1/1/2016
- BCD SOI = Bipolar, CMOS and DMOS on SOI – being removed on 1/1/2016
- BiCMOS = Bipolar and CMOS
- BiCMOS SOI = Bipolar and CMOS on SOI
- Bipolar = Bipolar
- CMOS = Complimentary Metal Oxide Semiconductor
- DRAM = Dynamic Randon Access Memory
- EEPROM = Electrically Erasable Programable Read Only Memory
- FDSOI = Fully Depelted Silicon On Insulator

- ImgSen = Image Sensor
- InterPos = Interposer
- MG = Multi-Gate (FinFET or TriGate)
- NAND = NAND Flash Memory
- NMOS = N type Metal Oxide Semiconductor
- NOR = NOR Flash Memory
- PDSOI = Partially Depeleted Silicon On Insulator
- SiGe = Silicon Germanium
- SRAM = Static Random Access Memory

Process details

- 100V = 100 volts
- 20V DMOS = 20 volts Double Diffused Metal Oxide Semiconductor
- 30V = 30 volts
- 30V DMOS = 30 volts Double Diffused Metal Oxide Semiconductor
- 40V DMOS = 40 volts Double Diffused Metal Oxide Semiconductor
- 500V DMOS = 500 volts Double Diffused Metal Oxide Semiconductor
- 5Vts = 5 threshold voltages
- 60V = 60 volts
- 60V DMOS = 60 volts Double Diffused Metal Oxide Semiconductor
- 650V DMOS = 650 volts Double Diffused Metal Oxide Semiconductor
- 65V DMOS = 65 volts Double Diffused Metal Oxide Semiconductor
- 80V = 80 volts
- 80V DMOS = 80 volts Double Diffused Metal Oxide Semiconductor
- Analog = Analog
- BSI = Backside Image Sensor
- Comp = Complimentary
- CPA = Common Platform Alliance
- DGO = Dual gate oxide
- DMOS = Double Diffused Metal Oxide Semiconductor
- DNW = Deep N-Well
- eDRAM = Embedded Dynamic Random Access Memory
- eFlash = Embedded Flash Memory
- FPGA = Field Programmable Gate Array
- FSI = Front Side Illuminated Image Sensor
- Fuse = Fuse
- Ge PMOS = Germanium P Type Metal Oxide Semiconductor
- HfO/AlO = Hafnium Oxide/Aluminum Oxide High-K Dielectric
- HKMG = High-k metal gate
- HKMIM = High-K Metal -Insulator-Metal Capacitor
- HV = High Voltage
- LV = Low Voltage
- MIM = Metal-Insulator-Metal Capacitor
- Mixed Sig = Mixed Signal
- NMOS = N Type Metal Oxide Semiconductor
- PMOS = P Type Metal Oxide Semiconductor

- PPCaps = Polysilicon to Polysilicon capacitors
- Pressure Sensor = Pressure Sensor
- RCAT = Recessed Access Array Transistor
- RDL = Redistribution Layer
- RF = Radio Frequency
- Res = a special mask to create a high value resistor
- Saddle Fin = Saddle FinFET Access Array Transistor
- Schottky = Schotty diode
- TFR = Thin Film resistor
- SiGe = Silicon Germanium
- Silk ILD = A Low-K Spin-On Interlevel Dielectric
- SVia - super via, a via that jumps past a metal layer to connect layer n + or - 2 instead of n + or - 1.
- TaN Res = Tantalum Nitride Resistor
- TGO = Triple Gate Oxide
- VNPN = Vertical P-Type/N-Type/P-Type Bipolar Transistor
- Vt = Threshold Voltage
- ZAZ = Zirconium Oxide/Aluminum Oxide/Zirconium Oxide High-K Dielectric

The easiest way to determine the process to use is to ask the supplier, many if not most of our customers are able to get enough information from the supplier to determine the process to use.

If the supplier will not provide the information you can check with us and see if we can help, but please keep in mind that there are hundreds of thousands of different semiconductors and we cannot be familiar with all or even most of them, please see our "Support Policy" for more information on how to determine what process to use and what help we provide.

If the supplier won't provide information and we are unable to help you can hire a company like TechInsights to do a tear down. A tear down will give you the node, process type, gates oxide, metal and poly layers. A tear down will not provide the wafer size.

In order to determine wafer size some general guidelines:

Wafer size	Typical process range
150mm	>500nm
200mm	<1,000nm, >90nm
300mm	<180nm

It is very unusual to see a 200mm process below 130nm although some NOR flash at 90nm and 65nm has occurred. If you see a process other than NOR Flash at 90nm or smaller you can be very confident it is on 300mm wafers. You can also look through the process dropdown in the model to see what wafers sizes and linewidths typically occur together.

If you need a process that is not currently supported in the model you can request one using our "add a process to the model form" and fill that out. As long as the requested process fits within the model description from page one and we have enough information we will add the process to the model. Please see our "Support Policy" for information on what processes we will add to each model.

Foundry volumes and margin

There are basically three kinds of companies in the semiconductor business:

- Integrated Device Manufacturer (IDM) – IDM's design their own products, fabricate the wafers, test them, package the parts, test them again and take them to market.
- Fabless – fabless companies design semiconductors but rely on other companies to fabricate the parts for them. They may or may not test the parts themselves and they typically outsource the packaging as well.
- Foundry – a company that owns their own wafer fabs and fabricates wafers for others.

If the process you select is an IDM process (the company in the process description is an IDM) then the foundry margin will be zero. This is because the company transfers the fabricated wafers internally and only takes a margin at the end when the finished part is sold. If you select a foundry process (the company in the process is a foundry) then the foundry will sell the wafers to the fabless semiconductor company with a margin added to it (some IDMs also buy at least part of their wafer requirement from foundries).

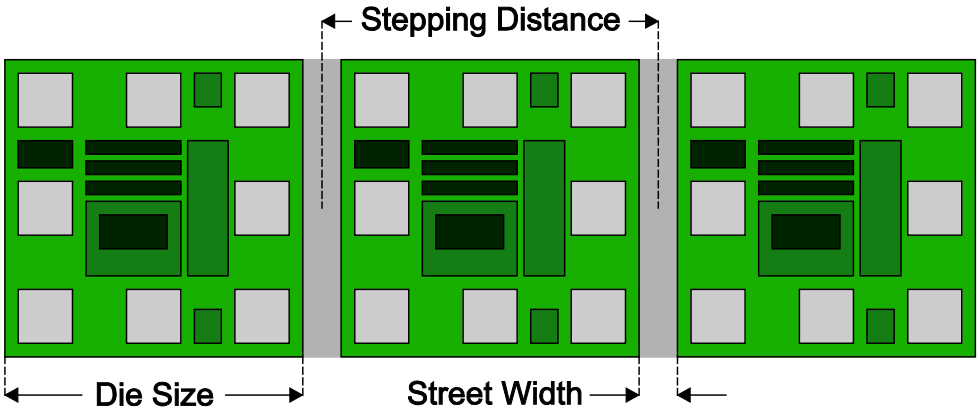
For each foundry process in the model we have an average gross margin for the foundry. The average margin is then adjusted based on the depreciation state of the fab and the volume being purchased.

The cost to make a wafer depends on the process, the wafer fab and how full the fab is. Unless a customer is so big that they largely determine how full a fab is the wafer cost is not sensitive to the customer volume, however, the margin is very sensitive to volume. The table (row 14) lists the volumes in wafers per month a company has to buy from the foundry to be a low, medium or high volume customer of the foundry. This volume is number of wafers of the wafer size selected for the process. This should reflect the total volume of wafers the company buys from the foundry, not just what they buy for a single product. Below the volume line the foundry margins in percentage are shown (row 15). Below this is a selection:

2.1) Select a foundry margin (cell D17) – if you select engineering the engineering margin will be added to the wafer cost, is you select low, average or high, the low average or high volume margin will be added to the cost. You can also directly choose a margin. If a non-foundry process has been chosen the margins are zero unless you directly select a margin. The resulting wafer price (cost + margin) is displayed in cell K17. If you are not sure what to select for margin, there is a foundry usage and margin lookup on the 'Lookups' sheet.

3.0) Enter the die size – in cells C14 and E14 the die length and width in millimeters should be entered. The model takes the die size, adds street width and calculates the exact number of whole die that will fit onto a wafer based on wafer size and edge exclusion. If a supplier will not tell you the die size (this is very unusual) and x-ray of the package can be performed or the package can be decapped to measure the die size. We recommend TechInisght for this service.

There is more than one way to describe die size and it is important to understand the differences. The following figure illustrates three die in a row on a wafer. Notice that there is the physical die size and then between each die there is a blank "street". The street provides an area for the saw cut used to separate the finished die. The model assumes that the die size that is entered is the physical die size of the die and by default the model adds a 75 micron street width when calculating the whole die on a wafer. Sometimes die sizes are specified using the stepping distance from the middle of a street to the middle of the next street. In this case you need to override the street width and set it to zero. Another situation that you may encounter is where a die size is measured after sawing, you need to make sure the measurement is the die only and not some remnant of the street still attached to the side of the die. The street is made wider than a typical saw cut to leave some room for misalignment and saw damage around the cut.



Die Size

Other factors to take into when determining the number of whole die on a wafer are the edge exclusion and die clustering.

- Edge Exclusion – due to issues with maintaining prefect process uniformity all the way to the edge of a wafer there is an edge exclusion area at the edge of the die where no good die exist. By default the model leaves a 2mm edge exclusion but you can override that if necessary on the 'Defaults' sheet.
- Die Clustering – virtually all fabs use stepper based exposure systems to print the patterns that build up ICs. The field of a stepper typically encompasses several die and then the field is stepped across the wafers. For gross die calculations it may be necessary to consider die clustering because the stepper field behaves like a big die with several die inside it. On the 'Defaults' sheet you can select various stepper (and scanner) field sizes to activate die clustering.

4.0) Select product type for test (cell C15) – the product type determines default test times and the type and cost for the test equipment. Many standard product types are pre-defined here.
- CMOS Image Sensors - select CIS and the number of pixels.
- Logic - if the device is a DSP, Embedded Processor, Microcontroller or Microprocessor simply select the appropriate device and configuration (number of cores, embedded memory, etc.). For all other logic devices select ASIC with the appropriate device performance and

complexity. To help with ASIC type selection there is an ASIC type lookup on the 'Lookups' sheet. See the section on 'Lookups' for how to use the ASIC lookup.

- Memory - for memory simply select the memory type: DRAM, NAND, NOR, SRAM and the memory density.
- Mixed Signal - ICs combining a significant amount of analog with digital are mixed signal. Select mixed signal and the appropriate complexity. We do not currently have help for selecting the complexity of mixed signal ICs.
- RF - RF testing is very expensive because of the frequencies involved. For RF products select RF with the appropriate complexity for the device We do not currently have help for selecting the complexity of RF ICs.

5.1) Assembly location/provider – this selection determines the country assembly is done in and the gross margin for determining the price.

5.2) Volume – this is the volume of assembly business the company does with the assembly provider and increases or decreases the gross margin applied to determine the price. If the company does <$100k per year of total packaging volume with a provider, the volume is very low, >=$100K to <$1M is low, >=$1M to <$10M is average, >=$10M to <$50M is high and >=$50M is very high.

5.3) Package Type – select “Leadframe” for leadframe type packages, “No packaging” if packaging isn’t performed, “Organic Substrate” for organic substrate packages, and “Wafer level” for wafer level packaging. **The selection you make here will grey out the selections below that aren’t used for the package type you select.** When you select “Leadframe”, selection 5.3.1 is active and turns white. If you select “No packaging” then selection 5.5.1 is active and turns white, if you select “Organic Substrate” then selections 5.4.1, 5.4.2, 5.4.3 and 5.4.4 are active and turn white. If you select “Wafer level” then selections 5.5 and 5.5.1 are active and turn white.

5.4) Leadframe configuration – if “Leadframe” is selected for 5.3, then this selection is active and turns white. Select the leadframe you want from the dropdown. If 5.3 is not set to “Leadframe” this dropdown is greyed out and doesn’t do anything. If you click on it anyway you will see the list, but the selection doesn’t drive the cost at all.

5.5.1) Organic Substrate Size - if “Organic Substrate” is selected for 5.3, then this section is active and turns white. Enter the height and width of the organic substrate. If 5.3 is not set to “Organic Substrate” this area is greyed out and doesn’t do anything. Please note the organic susbtartes size is also referred to as the “body size”.

5.5.2) Organic Substrate Layers - if “Organic Substrate” is selected for 5.3, then this section is active and turns white. Enter the number of core and build up layers. If 5.3 is not set to “Organic Substrate” this area is greyed out and doesn’t do anything. Layers may be determined by doing a side view x-ray of a package or by cross sectioning the package. We recommend TechInsight for package analysis. Also see the background section on layers later in this manual.

5.5.3) Organic Substrate Connection Type - if “Organic Substrate” is selected for 5.3, then this section is active and turns white. Select either “Flip Chip” or “Wirebond” for the ways the die is electrically connected to the substrate. If 5.3 is not set to “Organic Substrate” this area is greyed

out and doesn't do anything. Connection type may be determined by doing a side view x-ray of a package or by cross sectioning the package. We recommend TechInsight for package analysis.

5.5.4) Organic Substrate Connections - if "Organic Substrate" is selected for 5.3, then this section is active and turns white. Enter the number of package pins/balls. If 5.3 is not set to "Organic Substrate" this area is greyed out and doesn't do anything.

5.6) Wafer level configuration - if "Wafer level" is selected for 5.3, then this section is active and turns white. Select the wafer level packaging from the dropdown list. If 5.3 is not set to "Wafer level" this area is greyed out and doesn't do anything.

5.6.1) Bond pads - if "Wafer level" or "No packaging" is selected for 5.3, then this section is active and turns white. Enter the number of bond pads on the die. This is used to drive the product test costs". If 5.3 is not set to "Wafer level" or "No packaging" this area is greyed out and doesn't do anything.

Background – Cost Accounting

Cost accounting practices break out manufacturing costs in three categories:

1. *Material – material only includes materials that become part of the final product that is shipped. Materials consumed in product are included in overhead and do not count as materials.*
2. *Labor – labor only include direct or "touch" labor, basically the operators who make the product. Indirect labor such as engineers, technicians, managers and supervisors are included in overhead.*
3. *Overhead – everything else.*

The following table summarizes what is included in each category for different phases of IC production.

Category	***Wafer Fabrication***	***Packaging***	***Test***
Material	*Starting Wafer*	*Substrates, Leadframes, Wire, Mold Compound*	*None*
Labor	*Operators*	*Operators*	*Operators*
Overhead	*Depreciation, Equipment maintenance, Indirect labor, Monitor wafers, Facilities costs, Consumables*	*Depreciation, Equipment maintenance, Indirect labor, Facilities costs, Consumables*	*Depreciation, Equipment maintenance, Indirect labor, Facilities costs, Consumables*

Background - Wafer Cost Calculation

As previously described, cost accounting practices break up the cost to manufacture a product for sale into three categories, material, labor and overhead:

- *Material – material is confined to materials used to make the product that becomes part of the product that is shipped. Only if the material becomes a physical part of the product being shipped does it count in the material category. For wafer fabrication the only material is the starting wafer.*
- *Labor – labor in this case is restricted to direct labor sometimes referred to as touch labor. Direct labor is the labor cost for the operators who physically manufacture the product. Engineers, supervisors, technicians and managers do not count as direct labor and are included in the indirect labor category described below.*
- *Overhead – everything else required manufacturing the product. In the IC Knowledge cost models overhead is broken down into depreciation, equipment maintenance, monitor wafers, indirect labor, facilities and consumables.*

As previously described overhead is everything other than material (starting wafers) and labor (direct labor from operators) required to produce the product. The following is a further breakout and discussion of the various overhead sub categories:

- *Depreciation – equipment has a finite usable lifetime. The idea behind depreciation is to take the cost of a piece of equipment and write it off over the course of its useful life. For example if a piece of equipment costs one million dollar and has a useful lifetime of five years, two hundred thousand dollars would be charged to manufacturing cost each year for each of the first five years. In the semiconductor industry the useful life of some process equipment may be shorter than government regulations allow and furthermore regulations vary from country to country. Generally speaking the industry has settled on five year depreciation for process equipment when reporting results (although other rules may be used for tax purposes). The following are the default depreciation rates used in the cost models:*

Item	*Useful life*	*Depreciation rate*
Process tools	*5 years*	*20%*
Process tools installation	*5 years*	*20%*
Building systems (ultrapure water, gas and chemicals, cleanroom, HVAC)	*10 years*	*10%*
Automation	*10 years*	*10%*
Building structure	*15 years*	*7%*

The deprecation calculation is the cost of the item multiplied by the depreciation rate. This amount is charged to the manufacturing cost each year until the useful life is reached at which time the depreciation for that items goes to zero.

With expansions and upgrades there may be a wide variety of equipment ages in the same facility. The Cost Model provides for an initial equipment set and up to three upgrades/expansions and tracks each set individually.

- *Equipment Maintenance – the cost of parts and service contracts for the process equipment are captured in this category. The company employees such as technicians and engineers that maintain the equipment are not counted in this category. Equipment maintenance is calculated as a percentage of the original acquisition cost of the equipment used to estimate yearly maintenance costs.*
- *Indirect labor – engineers (both process and equipment), technicians (both process and equipment), supervisors and managers are all counted in this category. Indirect labor hour per mask layer are used to estimate total indirect labor hours. Total indirect labor hour are then broken down by type using "typical" fab indirect labor profiles and labor rates for engineers, technicians, supervisors and managers by country are used to calculate indirect labor costs.*
- *Monitor wafers – test wafers used to monitor the performance of equipment. These wafers are used to perform a test by running them through one or more process steps and then measuring the result. The wafers are then scrapped or reclaimed.*
- *Facilities – the cost of utilities (electricity, natural gas and water), ultrapure water generation, waste water treatment, facility maintenance (HVAC, Ultrapure water, gas and chemical systems), insurance, occupancy (cleaning and waste disposal), landscaping and telecommunications.*
- *Consumables – reticles, photochemicals, cleaning chemicals, etching and deposition gases, bulk gases, CMP pads and slurries, sputter targets, implant sources, deposition precursors, etc.*

Background – Wafer fab equipment depreciation

Due to the complexity of the wafer fab equipment calculations they bear a more detailed examination. The model allows a fab to have an initial equipment set and up to 10 upgrades. In each case when and what came online and how much it cost is tracked. The model also allows the user to adjust the depreciation period.

In the simplest example a wafer fab is built with an initial equipment set and is never upgraded. If for example a one billion dollar equipment set is put online, then by default $200 million dollars will be written off each of the first 5 years and in year 6 depreciation becomes zero. If a user were to change the depreciation to 7 years, then $143 million dollars would be written off each of the first 7 years and then go to 0 in year 8.

If a fab is less than 6 years, old the depreciation be default would be 20% per year, if you switch from 5 year to 7 year depreciation the depreciation would switch to ~14% decreasing the depreciation charges. If however the fab is 6 years old the depreciation would be 0 by default and if you switched to 7 year depreciation the depreciation would become ~14% increasing the depreciation cost. Once a sufficient amount of time has passed changing the length of depreciation has no effect because the equipment is fully depreciated in all cases.

If the fab has gone through multiple upgrades the situation gets a lot more complicated. For example, if a fab had an initial equipment set of $1 billion dollars and then each year had a $100 million dollar equipment upgrade for the first 5 years the deprecation would look like the following.

	Initial set	*Upgrade 1*	*Upgrade 2*	*Upgrade 3*	*Upgrade 4*	Upgrade 5	*Total*
Year 1	*$200M*	*$0M*	*$0M*	*$0M*	*$0M*	$0M	*$200M*
Year 2	*$200M*	*$20M*	*$0M*	*$0M*	*$0M*	$0M	*$220M*
Year 3	*$200M*	*$20M*	*$20M*	*$0M*	*$0M*	$0M	*$240M*
Year 4	*$200M*	*$20M*	*$20M*	*$20M*	*$0M*	$0M	*$260M*
Year 5	*$200M*	*$20M*	*$20M*	*$20M*	*$20M*	$0M	*$280M*
Year 6	*$0M*	*$20M*	*$20M*	*$20M*	*$20M*	$20M	*$100M*
Year 7	*$0M*	*$0M*	*$20M*	*$20M*	*$20M*	*$20M*	*$80M*
Year 8	*$0M*	*$0M*	*$0M*	*$20M*	*$20M*	*$20M*	*$60M*
Year 9	*$0M*	*$0M*	*$0M*	*$0M*	*$20M*	*$20M*	*$40M*
Year 10	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$20M*	*$20M*
Year 11	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*
Year 12	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*
Year 13	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*

Depreciation Versus Year.
5 Year depreciation, $1 billion dollar initial investment
and $100 million dollar upgrade each of the first 5 years.

The next table illustrates the depreciation for the same case except that the depreciation period is changed to seven years.

	Initial set	*Upgrade 1*	*Upgrade 2*	*Upgrade 3*	*Upgrade 4*	Upgrade 5	*Total*
Year 1	*$143M*	*$0M*	*$0M*	*$0M*	*$0M*	$0M	*$143M*
Year 2	*$143M*	*$14M*	*$0M*	*$0M*	*$0M*	$0M	*$157M*
Year 3	*$143M*	*$14M*	*$14M*	*$0M*	*$0M*	$0M	*$171M*
Year 4	*$143M*	*$14M*	*$14M*	*$14M*	*$0M*	$0M	*$186M*
Year 5	*$143M*	*$14M*	*$14M*	*$14M*	*$14M*	$0M	*$200M*
Year 6	*$143M*	*$14M*	*$14M*	*$14M*	*$14M*	*$14M*	*$214M*
Year 7	*$143M*	*$14M*	*$14M*	*$14M*	*$14M*	*$14M*	*$214M*
Year 8	*$0M*	*$14M*	*$14M*	*$14M*	*$14M*	*$14M*	*$71M*
Year 9	*$0M*	*$0M*	*$14M*	*$14M*	*$14M*	*$14M*	*$57M*
Year 10	*$0M*	*$0M*	*$0M*	*$14M*	*$14M*	*$14M*	*$43M*
Year 11	*$0M*	*$0M*	*$0M*	*$0M*	*$14M*	*$14M*	*$29M*
Year 12	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$14M*	*$14M*
Year 13	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*	*$0M*

Depreciation Versus Year.
7 Year depreciation, $1 billion dollar initial investment
and $100 million dollar upgrade each of the first 5 years.

Comparing the tables we can see that for the first five years the five year depreciation results in higher total depreciation costs, then for years seven through twelve seven year depreciation is higher.

In reality the situation is actually more complex than this with up to ten upgrades plus as upgrades take place some of the older equipment is removed and must be accounted for.

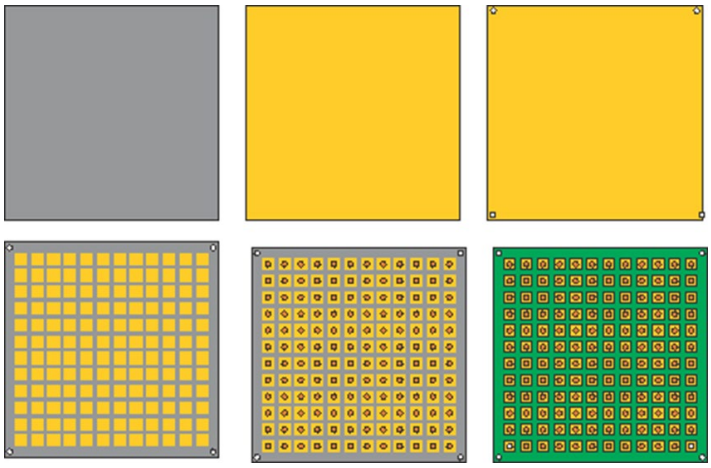
The model handles all of this accounting automatically and it isn't even visible to the user. If you feel you need to see the details of the equipment calculations and depreciation you need to purchase our strategic model where all of the calculation details are visible. We do not expose that detail in the IC model due to the audience the model is designed for.

Background – package layers

Organic substrate packages have layers to provide the ability to support a large number of connections.

The basic organic substrate fabrication process is:

1. *A sheet of glass fiber impregnated with BT resin.*
2. *Metalize the sheet.*
3. *Drill alignment holes.*
4. *Apply and pattern polyimide and metal runs.*
5. *Align and glue together multiple layers. Drill holes and plate to create metal filled vias.*
6. *Apply and pattern solder mask.*



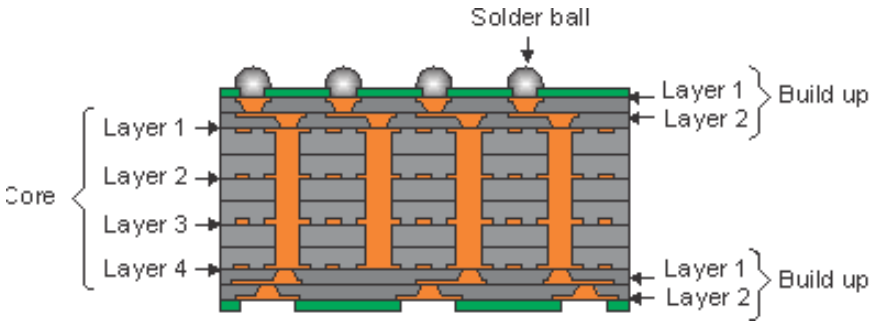
Organic substrate at the various steps in the fabrication process.

The number of layers created in this process are the organic substrate "core layers".

Built up substrates are used where greater precision is required than can be achieved by the process illustrated in the previous section.

Build up is very common for flip chips where pitches =< 100 microns are needed.

Build up utilizes deposited polyimide by screen printing or dry films followed by laser etching of vias and metal deposition and etching to "build up" layers on top of the core substrate.



Cross section of an organic substrate with 4 core layers and 2 build up layers.

Defaults (red tab)

The 'Defaults' sheet displays the default value for dozen of model setting and allows the user to override them. The default values are technology specific and many if not most user never need to adjust anything on this page.

In general, column D displays default values, column E allows the user to override the default and column F displays the final value used.

The 'Defaults' sheet is divided into sections by general area the defaults address.

Wafer Fab – these are setting that effect the wafer fab cost calculations.

- Utilization - The percentage of the fab capacity that is utilized. This has a huge effect on wafer cost with wafer cost going up as utilization goes down. The most common reason for changing this setting is described in the applications note "Using the IC Cost and Price Model to Estimate Foundry Wafer Cost and Price' available on the IC Cost and Price Model page on our web site. By default the model is set to 90% utilization because that is the utilization typically assumed when setting price.
- Country - The country the fab is located in. Changing the country changes the labor and utility rates.
- Wafer type – The starting wafer type. This is automatically filled in for the process selected on the 'Main Selections' sheet. Override values available include:
    - Polished - a bare unprocessed wafer.
    - Epi, a polished wafer with an epitaxial layer on it.
    - PDSOI (partially depleted SOI), SOI used for some older technologies (typically 40nm and above). Please note that selecting PDSOI will change the starting wafer cost but not adjust the process to reflect the differences in SOI versus bulk processing.
    - FDSOI-2D (fully depleted SOI) used for planar fully depleted SOI processes. Please note that selecting FDSOI-2D will change the starting wafer cost but not adjust the process to reflect the differences in SOI versus bulk processing.
    - FDSOI-3D (fully depleted SOI) used for some FinFET processes. Please note that selecting FDSOI-3D will change the starting wafer cost but not adjust the process to reflect the differences in SOI versus bulk processing.
- Mask set pre-paid – this setting determines whether the mask set cost is amortized into the wafer manufacturing cost. By default this is set to "No" for foundries and "Yes" for everything else. This is because mask sets are typically paid for as part of NRE for foundry processes and not included in the cost. You can override the vale to "No" for not amortized or "Yes" for amortized.
- Mask set usage (wafers/set) – sets the number of wafers a mask set is amortized over. This number depends on the product type and year. If 'Mask set pre-paid' is yes, this setting has no effect.
- Wafer yield (%) – the number of wafers finished through the wafer fabrication process divided by the number of wafers introduced into the wafer fabrication process. The default yield is calculated based on the number of mask layers in the process.
- Years to depreciate equipment over – equipment is depreciated using a straight line calculation over the number of years set here, by default this is set to five years. For 5 years 1/5 of the equipment is written off for each of the first 5 years, for 7 years 1/7 of the equipment value is written off each year for 7 years, etc. See the background sections on "Wafer cost calculation" and "Wafer fab equipment depreciation" to better understand this setting.

- Wafer cost override – when set to “Default” (column F) the wafer cost calculated by the model is used. If set to “User” (column F) the value entered is used (column E).
- Equipment set cost multiplier – the equipment set cost is multiplied by this value. By default, this is set to one.
- Wafer IP cost adder - if you select "user" in column f whatever intellectual property cost you enter in column E will be added to the wafer cost.

Gross and Net Die – these setting determine the number of whole die per wafer (gross die) and the number of good die after test (net die)

- Defect density (N/cm2) – the defects per unit area utilized to calculate the die yield (see the background on “Yield Models”). The high the defect density the lower the yield will be for a given die size. The default defect density depends on the process, year and quarter. Please note the default defect densities are for the Murphy model and if you select a different defect model you must enter your own defect density.
- Edge exclusion – wafer fabrication processes are not perfectly uniform to the wafer edge and there is an “exclusion” zone where no good die exist. This “edge exclusion” is subtracted from the wafer size to calculate the number of whole die that fit on the wafer.
- Die clustering – die are printed on the wafer using stepper systems where multiple die are printed at each time. This can cause the groups of die printed at the same time to behave like one large die instead of individual die when it comes to fitting the die on the wafer. Die clustering allows the user to set the die clustering so it is taken into account when calculating gross die.
- Street width – the area between die left empty to make a space for the wafer saw. See also “Die size” in the ‘Main Selections” sheet description.
- Yield model – the default yield model utilized to calculate the die yield is the murphy model. This setting allows the user to override the default yield model and select an alternative model. See the background on “Yield Models” following this section for a discussion of yield models.
- N for Bose Einstein – the Bose Einstein yield model requires a value for N to be entered. If you select Bose Einstein as the yield model in the previous setting you must enter N here. If any other model is selected this entry has no effect. See the background on “Yield Models” for more information.
- Die area breakout – this is a set of 8 setting that allows the user to calculate and use a defect density based on different defect densities for different areas of the die. The first four settings define the % of the die that is 3 different types of memory and logic. The sum of these four areas must be 100% or you will get an error. Changing these four setting doesn’t have any effect until you also change the defect densities for each of the 4 areas. By default the four areas all have the default defect density. You must go in and change this after you have selected the different area percentages. We do not have any data on defect densities for different memory areas and this is just a calculator for user convenience. You as a user are responsible for entering the areas and defect densities here.

Test – this section sets all of the defaults for wafer sort and class test.

- Product level – this is a very useful setting for companies involved in automotive, military and aerospace. By default this is set to commercial, when you switch to automotive, military or aerospace additional testing and documentation is activated.

- Sort equipment date on-line – the year the sort equipment came on-line. This is used for the equipment depreciation calculation. The default value is set by the '2 Select process to model' on the 'Main Selections' sheet.
- Sort test time (secs) – this is the time in seconds to test a single die. The default value is determined by the '4 Select product type for test' setting on the 'Main Selections' sheet. If you know the actual test time you should select it here.
- Sort parallel testing (units) – the number of units tested at the same time during sort. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Sort parallel efficiency (%) – the efficiency of units tested at the same time during sort. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet. This is used along with the number of units sorted in parallel to determine the adjusted test time. See the background "Parallel testing efficiency" after this section.
- Sort system cost ($/system) – this is the default of the sort tester and prober calculated by the model based on the product being tested.
- Sort country – this is the default country wafer sort is performed in. By default it is the same country that the fab is in.
- Sort utilization (%) – this is the percent of the uptime sort equipment is being used to process wafers. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Sort uptime (%) – this is the percent of the time sort equipment is up and available to process wafers. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Sort 1 time (% of sort test time) – sort may require multiple passes. This setting is the percentage of the sort test time that is used to test the die during the first pass. For some devices this may be the only test and the test time would be 100%. For other products, there may be multiple passes and test 1 might be only a partial test. The default depends on the'1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Wafer bake – for certain products types the wafers are sorted, then baked to weed out infant mortality and sorted again. This setting sets the bake time. The default depends on the 1'1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Memory repair – for certain memory parts after sort 1 the extra memory bits can be sued to repair a defective memory array by blowing fuses. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Sort 2 time (% of sort test time) – sort may require multiple passes. This setting is the percentage of the sort test time that is used to test the die during the second pass. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Sort 3 time (% of sort test time) – sort may require multiple passes. This setting is the percentage of the sort test time that is used to test the die during the third pass. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".

- Class equipment date on-line – the year the class equipment came on-line. This is used for the equipment depreciation calculation. The default value is set by the '2 Select process to model' on the 'Main Selections' sheet.
- Class test time (secs) – this is the time in seconds to test a single part. The default value is determined by the '4 Select product type for test' setting on the 'Main Selections' sheet. If you know the actual test time you should select it here.
- Class parallel testing (units) – the number of units tested at the same time during class test. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Class parallel efficiency (%) – the efficiency of units tested at the same time during class test. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet. This is used along with the number of units Classed in parallel to determine the adjusted test time. See the background "Parallel testing efficiency" after this section.
- Class system cost ($/system) – this is the default of the Class tester and handler cost calculated by the model based on the product being tested.
- Class test country – this is the default country wafer class test is performed in. By default it is the Philippines.
- Class test utilization (%) – this is the percent of the uptime class test equipment is being used to process wafers. The default depends on the 1'1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Class test uptime (%) – this is the percent of the time class test equipment is up and available to process wafers. The default depends on the 1'1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet.
- Class test yield – the percentage of units that pass class test. By default this is based on the product pins.
- Lot size – the number of parts in a lot. This setting only takes effect if the part is aerospace or military or you turn on one of the next eight settings, or final three settings: Internal visual ($), Nondestructive bond pull ($), Serialization ($), Temp cycle ($), Constant acceleration ($), Particle impact noise ($), Fine and gross leak test ($), Radiographic ($), Fine and gross leak test ($), External visual inspection ($), Documents ($).
- Internal visual ($) – the cost per lot to perform internal visual inspection. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Non-destructive bond pull ($) – the cost per lot to perform bond pull strength testing, this is not done to failure but rather to a minimum pull strength. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Serialization ($) – the cost per lot to serialize the parts. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Temp cycle ($) – the cost per lot to perform temp cycling. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".
- Constant acceleration ($) – the cost per lot to perform constant acceleration testing. The default depends on the '1 Select year and quarter to model' and '4 Select product type for test' settings on the 'Main Selections' sheet and the "Product level".

- Particle impact noise ($) – the cost per lot to perform particle noise impact testing. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Fine and gross leak test ($) – the cost per lot to perform fine and gross leak testing. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Radiographic ($) – the cost per lot to perform radiographic testing. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Pre burn-in test time (% of class test time) – Class test may require multiple passes. This setting is the percentage of the class test time that is used to test the product before burn-in. For some devices this may be the only test and the test time would be 100%. For other products, there may be multiple passes and this might only be a partial test. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Burn-in (hrs) – the number of hours the product is burned-in to weed out infant mortality. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Interim electrical (% of class test time) – Class test may require multiple passes. This setting is the percentage of the class test time that is used to test the product in between multiple burn-ins. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Burn-in (hrs) – the number of hours the product is burned-in to weed out infant mortality. This is a second burn-in. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Room test (% of class test time) – Class test may require multiple passes. This setting is the percentage of the class test time that is used to test the product at room temperature after burn-in(s). The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Hot test (% of class test time) – Class test may require multiple passes. This setting is the percentage of the class test time that is used to test the product at high temperature after burn-in(s). The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Cold test (% of class test time) – Class test may require multiple passes. This setting is the percentage of the class test time that is used to test the product at cold temperature after burn-in(s). The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Fine and gross leak test ($) – the cost per lot to perform fine and gross leak test. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.

- External visual inspection ($) – the cost per lot to perform external visual inspection. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.
- Documents ($) – the cost per lot for documents. The default depends on the ’1 Select year and quarter to model’ and ‘4 Select product type for test’ settings on the ‘Main Selections’ sheet and the “Product level”.

Assembly and Packaging – default settings for assembly and packaging

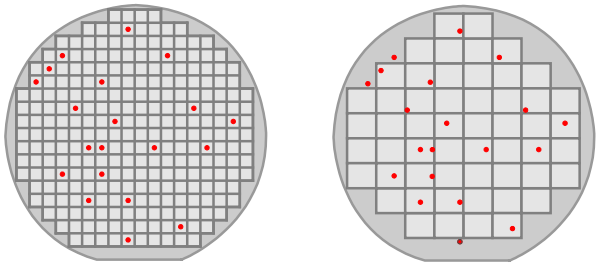
- Assembly yield – the percentage of parts completed through assembly divided by the parts started into assembly. The default is calculated based on the number of pins.
- Wire bond type – select between aluminum, copper or gold wire. Please note this default is only active for die that are connected by wire bonds.
- Bypass capacitors (#) – some products have bypass capacitors included in the package. Select the total number of bypass capacitors here.
- Power supply capacitors (#) – some products have power supply capacitors included in the package. Select the total number of power supply capacitors here.
- Package cost override – by default (default in column F) the calculated packaging cost is used in the model. If you select “User” (column F), then the user entered value (column E) is used.
- Package IP adder - if you select "user" in column f whatever intellectual property cost you enter in column E will be added to the package cost.

Product - default settings for the overall product.

- Product IP adder - if you select "user" in column f whatever intellectual property cost you enter in column E will be added to the product cost.

Background – Yield Models

Yield models are based on a simple concept that there are a specific number of random defects on each wafer that can cause a die to fail test. The higher the defect density but also the larger the die (see the figure)



20 Defects
20 Bad Die
264 Gross Die
92% Yield

20 Defects
16 Bad Die
54 Gross Die
70% Yield

Defect Density and Yield

As you can see from the figure, for an identical pattern and number of defects the yield is lower for larger die. This concept is mathematically expressed by defect models described below.

The model supports Bose-Einstein, Exponential, Murphy, Poisson and Seeds Yield models. The mathematics and resulting yields for each model are:

Bose-Einstein

$$Y = \frac{1}{(1 + AD)^N}$$

Exponential

$$Y = \frac{1}{1 + AD}$$

Murphy

$$Y = \left[\frac{1 - e^{-AD}}{AD}\right]^2$$

Poisson

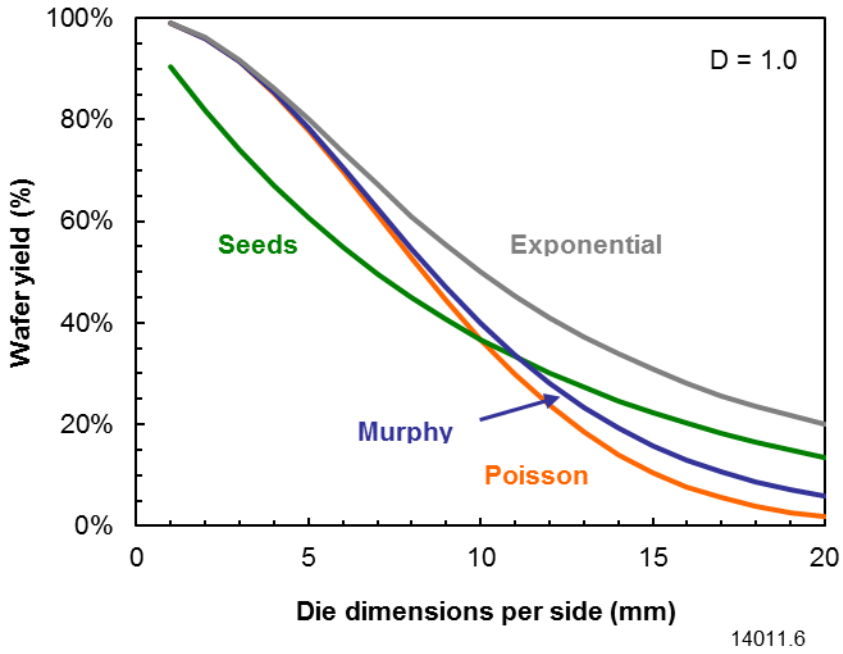
$$Y = e^{-AD}$$

Seeds

$$Y = e^{-\sqrt{AD}}$$

Where: A is the area, D is the defect density and N is the number of mask layers.

A comparison of the models for a value of D=1.0 is shown in the following figure:



Please note that the model default is the Murphy Model and all of the default defect densities are based on a Murphy Model. If you switch to a different yield model you must enter your own defect density that is appropriate for the model you have chosen.

Die yield in the model is based on defect density and die size. Defect density depends on the year and quarter you select to model in '1 Select a Year and Quarter to Model' and the process you select in '2 Select a Process to Model". For each process there are defect density values by quarter. Typically defect density is high for a process when it is first introduced and then defect density improves over time until steady state "mature" defect densities are achieved.

Background - Parallel testing efficacy

Testing multiple devices in parallel is an important technique for reducing test costs by spreading expensive test hardware costs out over more units. However, the more units tested in parallel the longer the test time characterized by the test efficiency given by the following formula.

$$M = 1 - \frac{(T_N - T_1)}{(N-1)T_1}$$

Where T_1 is the time to test one unit, N is the number of units tested in parallel and T_N is the test time for N units.

The ITRS has defined M and N by product and by year and we use those values to calculate the test time in parallel based on our estimates of T_1.

Background – Test and Burn-In Usage

Testing of integrated circuits is typically performed at wafer level as wafer sort or probe and at product levels as class or final test.

At wafer sort testing is typically single pass testing with the exception of Flash where testing is done followed by wafer bake and then a second testing pass. The two testing passes enable the number of units that went bad during wafer bake to be calculated. Automotive product testing may require multiple tests at different temperature, for example hot, cold and room temperature. For automotive multiple temperature testing in sort would be for die that will be used as flip chips in modules or other die used directly. If the die will go through the normal packaging process, then multiple temperature testing would likely be deferred until class test.

At class test products are typically tested, burned-in and tested again with the exception of lower end parts that are single pass tested with no burn-in. Automotive parts may once again be tested hot, cold and at room temperature. Aerospace and Military add additional test and inspections.

Background - Parallel testing efficiency

Testing multiple devices in parallel is an important technique for reducing test costs by spreading expensive test hardware costs out over more units. However, the more units tested in parallel the longer the test time characterized by the test efficiency given by the following formula.

$$M = 1 - \frac{(T_N - T_1)}{(N-1)T_1}$$

Where T_1 is the time to test one unit, N is the number of units tested in parallel and T_N is the test time for N units.

The ITRS has defined M and N by product and by year and we use those values to calculate the test time in parallel based on our estimates of T_1.

Cost Summary (brown tab)

The cost summary sheet summarizes all of the cost results from the model. This page is not user editable except a few white areas where previous results can be pasted for comparison purposes.

General information

Rows 7 through 14 display information related to the wafer fab and model. The date to model and current process are from the '1 Select year and quarter to model' and '2 Select process to model' selections on the 'Main Selections' sheet. The masks, fab name, fab on-line and process on-line dates, country and capacity are all the defaults for the fab associated with the '2 Select process to model'. The utilization is 90% by default unless overridden on the 'Defaults' sheet. Cell E14 also displays an information message if any defaults have been overridden.

Wafer Cost

Rows 17 through 28 break out the wafer fabrication cost into the major cost categories (see background Wafer Cost Calculation for more information). Column B lists the categories, column C has the annual costs for the entire fab in millions of dollars, column D has the costs in dollars per wafer, column E has the percentage of the total for each category, column F allows the user to paste results for comparison purposes. This is useful for understanding what the differences in costs are between two processes. You paste the results from one process, then select a different process and you can compare the cost by category between the two to understand what is different. Column G presents the results in dollars per square centimeter, column H presents the costs in dollars per mask and finally in column I the blended average depreciation rate for all of the different equipment sets is displayed (see background Wafer fab equipment depreciation).

The "Wafer fab IP and bumping adders" shows the cost for any wafer fab IP added on the 'Defaults' sheet and also if "Wafer Bumping" is selected on the 'Process Adders" sheet the cost is added here. "Wafer Bumping" on the 'Process Adders' sheet should only be used if wafers are purchased bumped from a foundry, for wafer bumping as a packaging option select one of the wafer bumping options in " 6 Select package type" on the 'Main Selections' sheet.

Process adders

Rows 31 through 55 indicate whether any process adders are active and if so which ones. There is also a pie chart of the wafer cost by category.

Wafer selling price

In rows 58 and 59 the foundry gross margin percentage (if any), foundry margin dollars (if any) and resulting selling prices (wafer cost plus foundry margin) are displayed. Please note that there is no foundry gross margin unless the process selected is a foundry process. IDMs transfer wafers internally at cost.

General information

In rows 62 and 63 the product type and die size are displayed.

Die cost

Rows 66 through 72 display the die cost elements.

- Gross die - depends on die size, wafer size, edge exclusion and street width. This is the number of whole die that fit on the wafer.

- Die yield - depends on the year and quarter and process. Die yield is the percentage of die that pass electrical test and are "good" usable die.
- Net die - gross die multiplied by die yield.
- Wafer sort cost - depends on the product type, die size, wafer size and number of package pins (package pins determines how many connections the test equipment has too accommodate at both wafer sort and class test) plus test related factors from the 'Defaults' sheet like parts tested in parallel, number of test passes, wafer bake, test equipment cost, wafer sort country, etc. This is the cost to test the wafer.
- Tested wafer cost - the yielded wafer cost plus foundry margin plus wafer sort cost.
- Cost per good tested die - tested wafer cost divided by net die.

Product information
Row 75 displays the package type and number of package pins.

Product cost
Rows 78 through 85 display the product cost.

- Assembly yield - the percentage of parts that complete assembly passing the assembly measurements and inspections.
- Package and assembly cost - the cost to assemble die into packages.
- Package IP adder - any packaging related intellectual property costs.
- Packaged die cost - for outsourced packaging this is the goo tested die cost divided by the assembly yield plus the packaging and assembly cost and package IP adder cost. The assembly yield is only applied to the die because companies only pay for good packages. If the packaging is done in-house, then the cost is the good tested die post plus the package and assembly cost plus the package IP adder all divided by the assembly yield.
- Class test cost - depends on the product type and number of pins as well as class test related factors from the 'Defaults' sheet such as parts tested in parallel, number of test passes, test equipment cost, country, etc. Class test cost is the final test of the packaged part.
- Class test yield - the percentage of packaged parts that pass class test.
- Product IP adder - the cost of intellectual property at a product level.
- Product cost - the packaged die cost plus class test cost plus product IP adder all divided by the class test yield.

The background ‘Product cost calculation’ following this section explains the calculations.

Selling price
Rows 88 through 103 display the selling price of the product versus margin and also present a pie chart breaking out product cost into major categories by percentage. The ‘Background – Gross Margin‘ and ‘Background – Cost and Price’ following this section have information on gross margin. There is also a ‘Gross Margin; lookup on the ‘Lookups’ tab.

Background – Product Cost Calculation

The product cost calculations are made as follows:

The packaged die cost calculation is by default based on packaging being performed by an outside contractor (this default may be changed on the 'Defaults' worksheet. When an outside contractor is used the contractor is only paid for good packages.

Packaged die cost = cost per tested good die/packaging yield + package cost

If the default is changed to in-house packaging then:

Packaged die cost = (cost per tested good die + package cost)/packaging yield

Product cost is calculated by:

Product cost = (packaged die cost + class test cost)/class test yield

Background – Gross Margin

Gross margin is the selling price minus the cost of goods sold. Gross margin percentage is the gross margin divided by the selling price for example:

If a product has a cost of goods sold (COGS) of $0.70 and sells for $1.00, then the gross margin (GM) is $0.30 making the gross margin 30%.

To convert from COGS to selling price for a given GM% use the following:

GM%	*Divisor*
20%	*0.80*
30%	*0.70*
40%	*0.60*
50%	*0.50*
60%	*0.40*
70%	*0.30*

For example, if COGS is $1.40, then a 60% GM would give a selling price of $3.50. A number of our customers have incorrectly made these calculations.

Background – Cost and Price

Cost is what it costs to make a product; price is what the market is willing to pay for the product. If you produce and sell a product the hope is always that the price will be greater than the cost by a significant margin but this is not always that case. Profit is gross margin minus below the line costs such as research and development, and general, selling and administrative Gross margins need to typically be greater than the high teens percentage to actually make a profit.

Price = cost + gross margin

If the cost is known (and that is primarily what this model calculates) and gross margin is known or can be estimated, then selling pricing is known and or can be estimated.

Foundry Margin

For foundry processes this sheet displays a graph of approximate foundry margin versus wafer volume for the specific foundry selected.

Cost Per Quarter Macro

This sheet allows a Macro to be run that populates a table of costs by quarter for twenty quarters. The cost sections include process details, wafer costs, foundry margin, gross and net die and die cost and packaging and class test costs.

To use the sheet:

1. Select a process on the 'Main Selections' sheet under '2 Select a process to model'.
2. In row 12 on the 'Cost Per Quarter Macro' sheet select ten quarters to model in cells D12 through W12. Please note all of these quarters must be after the process came on line or you will get errors when the table populates.
3. Press the rose colored "Run Macro" button on the sheet.

In order for the Macro to run the 'Cost Per Quarter Macro' sheet is unlocked. There are hidden cells on the sheet and if you overwrite them you will break the model. Only make selections in row 12 and copy results from the sheet, changing any other areas on the sheet may break the model.

Lookups (gray tab)

The lookups sheet provides six lookups to help determine what value to use elsewhere in the model. The lookups page suggests values to use but doesn't drive the model results.

Foundry usage

Select a company and node from the dropdown and the foundry used, comments, and foundry volume are displayed. This lookup helps with '2 Select a process to model' and the '2a Select a foundry margin' selections on the 'Main Selections' sheet.

Die size

Select the company and product from the dropdown and the die size is displayed. This lookup helps with the '3 Enter the die size' entry on the 'Main Selections' sheet.

ASIC test type

This lookup gives a rough idea of what ASIC test type to select in the '4 Select product type for test' dropdown on the 'Main Selections' sheet. You select the node and also select a die area that is the next larger size than your die. For example, if you die is 100mm^2, then it is bigger than 64mm2 and smaller than 128mm^2 so you pick 128mm^2.

Package type

This lookup helps with '5 Enter the number of package pins', '6 Select package type' and '8 Select package layers' on the 'Main Selections' sheet. Select the company and product type from the dropdown and the package type, package pins and layers are displayed.

Gross margin

Select a company from the dropdown and the companies average gross margin is displayed for the last 5 years and a 5 year average is also displayed.

Selling price

This is a calculator for selling price. The product cost calculated by the model is automatically filled in, you can then enter a gross margin and a selling price is displayed. You can also enter a product price and volume and have a price volume curve displayed. This is useful for example if you go on a distributor site and get a one thousand (1k) piece price, you can enter that price and see what the price will be at higher volumes.

Errors (gray tab)

In the event of an error in the model the type of error is displayed on this sheet.

If the error is “The wafer fab doesn’t exist yet” simply select a later date on the ‘1 Select the year and quarter to model’ selection on the ‘Main Selections’ sheet.

Errors due to 'Undefined material in the wafer cost engine' do not typically affect the cost much. You should notify us when you see an error but the model costs are likely still usable.

Generally speaking, all other errors will require you to notify IC Knowledge so that we can fix the error. Ideally you should send us the model set up exactly as it was when the error was triggered so that we can trouble shoot it.

Process Adders (blue tab)

The 'Process Adders' tab allows the user to modify a base process to include additional features.

- Al bond pads (yes/no) – adds an aluminum bond pads for wire bonding of copper metallization.
- Aluminum redistribution layer (yes/no) - adds an aluminum redistribution layer for flip chip bumping. This selection should only be used if the process is done in the fab as opposed to at a packaging house in which case the bumped die with RDL settings should be used in the "6 Select package type" on the 'Main Selections' sheet.
- Dual strain layers (yes/no) – adds dual strain layers.
- Embedded DRAM (stacked cell) (yes/no) – adds a stacked DRAM embedded DRAM.
- Embedded Flash (SONOS >=65nm)(+3 masks) (yes/no) adds a SONOS embedded Flash process appropriate for >=65nm node processes.
- Embedded Flash (SONOS 55nm)(+4 masks) (yes/no) adds a SONOS embedded Flash process appropriate for 55nm node processes.
- Embedded Flash (SONOS 40nm)(+5 masks) (yes/no) adds a SONOS embedded Flash process appropriate for 40nm node processes.
- Embedded Flash (ST Micro type - >40nm) (+10 masks, +1 poly) (yes/no) – adds an embedded Flash process similar to one ST Micro uses. This can be added to any process but is most relevant between 40nm and 130nm.
- Embedded Flash (SST SuperFlash ESF2 - 110nm to 250nm) (+9 masks, +3 polys) (yes/no) – adds SST SuperFlash ESF2 to a process. ESF2 is most relevant between 110nm and 250nm.
- Embedded Flash (SST SuperFlash ESF3 - <110nm) (+11 masks, +4 polys) (yes/no) – adds SST SuperFlash ESF3 to a process. ESF3 is most relevant below 110nm.
- Embedded MRAM (yes/no) - adds embedded MRAM memory.
- Extension/halo implants (add or subtract) – adds or subtracts extension/halo masks and implants. If you subtract too many extension/halos you will trigger an error that will display in column E, you then need to reduce the number of extension/halos you are subtracting.
- Ferric Inductor (yes/no) - adds a ferric inductor.
- Fuse (yes/no) – adds a fuse typically used for memory repair.
- High resistance poly resistor (yes/no) –adds a high resistance polysilicon resistor. This is a common adder for analog processes.
- Local interconnect - add a tungsten local interconnect mask and associated processing.
- Masked gate oxides (additional) – adds additional gate oxides. This block uses a mask to etch away gate oxide in a localized area and grow and additional thickness. You can 1 or 2 additional gate oxides.
- Metal layers (additional) – adds additional metals layers. You can add 1 to 4 additional metal layers.
- MIM Capacitors (yes/no) – adds an MIM capacitor. MIM caps are common in analog and RF processes.
- Polyimide layer - adds a 10 micron thick patterned polyimide layer plus the mask required to pattern the layer.
- Raised Source/Drain - (additional) – adds raised source/drains. You can add 1 or 2.
- Source/Drain contacts (add or subtract) – adds or subtracts source drain masks and implants. If you subtract too many source/drain contacts you will trigger an error that will display in column E, you then need to reduce the number of source/drain contacts you are subtracting.
- Stress memorization (yes/no) – add stress memorization.

- Thin film resistors (yes/no) – adds thin film resistors. This add on is most commonly used in analog or RF applications.
- Through silicon via (yes/no) – adds a via middle through silicon via to the process.
- Vt adjusts (add or subtract) – add or subtract Vt adjust masks and implants to the process. If you subtract too many Vt adjusts you will trigger an error that will display in column E, you then need to reduce the number of Vt adjusts you are subtracting.
- Wafer bumping (yes/no) - adds wafer bumping. This selection should only be used if the process is done in the fab as opposed to at a packaging house in which case the bumped die settings should be used in the "6 Select package type" on the 'Main Selections' sheet.
- Well (additional) – adds well masks and implants to the process. You can add from 1 to 4 additional wells.

Multiple Die Calculator (blue tab)

The multiple die worksheet allows any combination of multiple die in a package to be calculated. Die mounted side by side or stacked can both be calculated.

- Enter cost per good tested die from 'Cost Summary' sheet (row 7) – This line allows die costs for up to 7 different die to be entered. Use sheet 'Main Selections' sheet to calculate the cost of each die individually and then enter the values on this line from left to right. For each die enter the number of bond pads on the die as the package pins on the 'Main Selections' worksheet. Make sure 0 is entered for any die not used. The model counts non-zero values to determine the number of die.
- Enter gross margin if die is purchased (row 8) – for any die that are purchased enter the gross margin here. For any die that are not purchase lave the gross margin at 0%.
- Die cost with margin (row 9) – the die cost from row 7 with the margin from row 8 added. This value is calculated from rows 7 and 8 and is not user editable.
- Total tested die cost (row 10) – displays the total cost of all the die entered on row 7. This value is not user editable.
- Enter the package cost (row 11) – use the 'Main Selections' sheet to calculate a package cost. This is the base package cost with a single die. The cost will be adjusted for multiple die by the worksheet. Please note that the package cost also depends on the number of package pins entered on the 'Main Selections' worksheet and this number should reflect the total pins for the package when calculating the package cost. This value must be entered by the user.
- Package cost adjusted for multiple die (row 12) – displays the packaging cost adjusted based on the number of die in the package. The number of die is determined by the number of cells that have positive values on row 7.
- Enter package yield (row 13) – enter the packaging yield from the 'Cost Summary' worksheet when you calculated the package cost. This yield is for a single die package. It will be adjusted based on the number of die by the worksheet. This value must be entered by the user.
- Package yield adjusted for stacked die (row 14) – displays the yield adjusted for the number of die in the package. The number of die is determined by the number of cells that have positive values in row 7. This value is not user editable.
- Add package IP ($/part) (row 15) - enter any packaging intellectual property royalties per package here.
- Packaged die cost (row 16) – the total cost of the die and packaging adjusted for number of die and packaging yields. This value is not user editable.
- Enter class test cost for each die (row 17) – for each different type of die in the package calculate the test cost using the 'Main Selections' worksheet. Make sure as you calculate each one that the package pins is set to the number of bond pads on the die this corresponds to. These values (one for each die) must be entered by the user.
- Enter class test yield for each die (row 18) - for each different type of die in the package enter the test yield from the 'Cost Summary' worksheet. Make sure as you calculate each one that the package pins are set to the number of bond pads on the die this corresponds to. These values (one for each die) must be entered by the user.
- Total Class test yield (row 19) – the total class test yield for the product based on combining the yields of all of the individual die in the package. This is not user editable.
- Add product IP ($/part) (row 15) - enter any product intellectual property royalties per package here.

- Finished packaged part cost (row 21) – the total cost for the complete assembly with all of the die, testing and packaging costs and yields. This is not user editable.
- ***Selling price*** – rows 24 through 37 display selling prices for the part calculated on this sheet versus various gross margins.

Wafer Cost Detail (brown tab)

This sheet presents some additional details around the wafer fabrication process costs.

Cell C6 displays the mask set cost.

Rows 8 through 29 display the approximate number of tools and costs still on-line (after all of the upgrades the fab has undergone). These are approximate values, for detailed and exact values we recommend our Strategic Cost Model.

Rows 31 through 50 display approximate materials costs by category for the current process. These are approximate values, for detailed and exact values we recommend our Strategic Cost Model.

Row 52 through 61 display facilities costs for the wafer fab.

Override (red tab)

Most users never need to touch this worksheet. This worksheet is only needed if you want to control the model using other calculations or modeling results.

This worksheet allows the user to directly control the model by directly linking to the eight major model settings. For each setting if the value is set to 0 the values entered on the 'Main Selections' sheet are used. If the value is not zero the entered value overrides the values on the 'Main Selections' sheet. This allows calculation performed on the blank sheets to drive the model results. For each setting the 'List' sheet lists what each numeric value corresponds to.

- 1 Year and quarter to model – enter a number other than zero here and the value used in the model will be the value from the 'Lists' sheet.
- 2 Process to model – enter a number other than zero here and the value used in the model will be the value from the 'Lists' sheet.
- 2a Foundry Margin - enter a number other than zero here and the value used in the model will be the value from the 'Lists' sheet.
- 3 Die length – enter a number here other than zero representing the die length in millimeters and the entered value will be used in the model.
- 4 Die width – enter a number here other than zero representing the die width in millimeters and the entered value will be used in the model.
- 5 Product type – enter a number other than zero here and the value used in the model will be the value from the 'Lists' sheet
- 6 Package pins – enter a number other than zero representing the number of package pins and the entered value will be used in the model.
- 7 Package type - enter a number other than zero here and the value used in the model will be the value from the 'Lists' sheet
- 8 Package volume - enter a number here other than zero and the value used in the model will be the value from the 'Lists' sheet
- 9 Layers - enter a number here other than zero and the value used in the model will be the value from the 'Lists' sheet
- 10 Product level - enter a number here other than zero and the value used in the model will be the value from the 'Lists' sheet