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IC Knowledge - Strategic Cost Model Processes

Introduction

With the success of our Strategic Cost Model we are seeing an increasing number of our IC Cost and Price Model customers buying the model either as a companion to the IC Cost and Price Model or to replace the IC Cost and Price Model. For IC Cost and Price Model customers, it is important to understand the many differences in how the IC and Strategic Model's handle process definition.

IC Cost and Price Model Processes

In the IC Cost and Price Model processes are defined with the following nomenclature:

The syntax is: wafer size – node – company name – company process name (if applicable) – process type – process details (if applicable) – poly layers – metal layers/type

Even for the same wafer size, company, and node there may be many variants of a process by name and or metal layers. For example, at 28nm the model supports TSMC's: HP (G), HPC, HPL, HPM, and LP variants and in each case, has 7, 8, 9, 10 and 11 metal layers.

For each process in the IC model a specific fab is assumed for the process. The user cannot see the process details, the user can't directly edit the process and the user can't change the default fab.

The IC Cost and Price Model is also limited to processes in production now or expected to enter production in the next twelve months.

Strategic Cost Model Coverage

The Strategic Cost Model is a forward-looking model that includes process projections out as far into the future as we believe we can reasonably project. The model covers 2D and 3D NAND, 3D XPoint, DRAM and both foundry and IDM logic. For each product segment, we cover up to three leading companies. The companies covered in each segment are listed in table 1.

Product Category	Companies covered
2D and 3D NAND	Samsung, Toshiba, Intel-Micron
3D XPoint	Intel-Micron
DRAM	Samsung, Micron, SK Hynix
Foundry logic	TSMC, Samsung, Global Foundries
IDM logic	Intel, ST Micro

Table 1. Product categories and companies covered.

Due to the structure of the model and certain resource limits, the ability to add additional companies and segments is limited. Although we welcome customer suggestions about additional companies and segments to cover we do not add processes, companies or segments by customer request the way we do for the IC Cost and Price Model.

The Strategic Cost Model is primarily a 300mm model. There is some limited ability to model 200mm and 450mm in the model but the pre-defined options are all 300mm.

Fab Definitions

Unlike the IC Cost and Price Model where modeling begins by selecting a process the Strategic Cost Model - modeling process begins by selecting a wafer fab. Every 300mm fab for the companies and segments listed in table 1 is pre-defined in the model.

Specifically:

- Global Foundries - Fab 1 phases 1, 2 and 3, Fab 7, Fab 8 module 1 phases 1, 2 and 3, module 2 and 3, Fab 10 and Fab 11.
- Intel-Micron Flash - Fab 2, Fab 6 - Flash, Fab 10N, Fab 10N-3D, and Fab 10X.
- Intel - Fab 11X phases 1 and 2, Fab 12, Fab 24, Fab 32, Fab 42, Fab 68, Fab D1C, Fab D1D, Fab D1X phases 1 and 2.
- Micron - Fab 6 - DRAM, Fab 7, Fab 15, and Fab 16.
- SK Hynix - C2, M10 and M14 (DRAM).
- Samsung - Line 2, Line 11, Line 12, Line 13, Line 15, Line 16 phase A and B, Fab 17 phases 1, 2, 3 (S3-1) and 4 (S3-2), S1 phases 1, 2, and 3, S2 phases 1 and 2, Xian phases 1 and 2.
- ST Micro - Crolles II.
- Toshiba - Fab 3, Fab 4, Fab 5, and Fab Y2.
- TSMC - China, Fab 12 phases 1, 2, 3, 4, 5, 6, and 7, Fab 14 phases 1, 2, 3, 4, 5, 6, 7, 8, 9, and 10, and Fab 15 phases 1, 2, 3, 4, 5, 6, and 7.

For each of these fabs a table of the initial and up to ten upgrade configurations are visible and user editable. For each fab "state" the year and quarter, process, capacity and wafer size are listed. The model also supports up to five user defined fabs.

By starting with a fab selection users can explore differences in cost by fab and also get detailed equipment and materials requirements by fab.

Process Definitions

Unlike the IC Cost and Price Model where there may be many process variants for each node. the Strategic Cost Model has one variant per node. In the Strategic Cost Model, the process flows are visible for each process and the user can edit the flows to create different variants but it is up to the user to make the appropriate modifications.

The following base processes are pre-defined in the model:

- Global Foundries - 130nm G, 90nm G, 65nm G, 40nm G, 28nm HPP, 22nm FDX, 14nm LPP, 12nm FDX, 7nm LP, 7nm LPP, 5nm FF, 3.5nm HNW, 2.5nm CFET.

- Intel-Micron - 3DNAND 32L, 64L, 96L, 128L, 256L. 3D XPoint 25nm 2L, 20nm 4L, 16nm 8L, 16nm 16L.
- Intel - 130nm MPU, 90nm MPU, 65nm MPU, 45nm MPU, 32nm MPU, 22nm MPU, 22nm FFL, 14nm MPU, 10nm MPU, 7nm MPU, 5nm MPU.
- Micron - 2D NAND 90nm, 72nm, 56nm, 43nm, 32nm, 25nm, 20nm and 16nm. DRAM 110nm, 95nm, 78nm, 68nm, 58nm, 50nm 42nm, 31nm, 25nm, 20nm, 18nm, 14nm and 10nm.
- SK Hynix - DRAM 120nm, 80nm, 66nm, 54nm, 44nm, 30nm, 26nm, 20nm, 18nm, 14nm, and 10nm.
- Samsung - 2D NAND 120nm, 90nm, 75nm, 65nm, 51nm, 42nm, 35nm, 27nm, 21nm, 19nm, 16nm, 14nm. 3D NAND 24L, 32L, 48L, 64L, 128L, 256L. DRAM 150nm, 130nm, 110nm, 90nm, 80nm, 68nm, 58nm, 48nm, 32nm, 26nm, 20nm, 18nm, 14nm, 10nm. Foundry 90nm, 65nm, 45nm, 32nm, 28nm LPH, 28nm FDS, 20nm, 18nm FDS, 14nm LPP, 10nm LPP, 8nm LPP, 7nm LPP, 6nm LPP, 5nm LPP, 4nm LPP.
- ST Micro - logic processes 130nm, 90nm, 65nm, 45nm, 28nm LP, 28nm FDSOI.
- Toshiba - 2D NAND 90nm, 70nm, 56nm, 43nm, 32nm, 24nm, 19nm 1x, 19nm 1y, 16nm 1z. 3D NAND 24L, 48L, 64L, 96L, 128L, 256L.
- TSMC - logic processes 250nm, 180nm, 130nm, 90nm, 65nm, 40nm G, 28nm HP, 22nm ULP, 20nm SOC, 16nm FF+, 12nm FF, 10nm FF, 7nm FF, 5nm FF, 3.5nm HNW, 2.5nm CFET.

Some of the abbreviation above are specific company process designations. In general FF = FinFET, HNW = Horizontal Nano Wire (nano wire or nano sheets), CFET = Complimentary FET (stacked n and p type nanowires or nanosheets.